7050
DIGITAL
MULTIMETER

MP MASTER
MA24044

Schlumberger

TECHNICAL DATA

535

7050
DIGITAL
MULTIMETER

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7050
DIGITAL MULTIMETER

Date of Issue : May 1974

Schlumberger

THE SOLARTRON ELECTRONIC GROUP LIMITED
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TECHNICAL MANUAL

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SECTION 1 General

INTRODUCTION

The 7050 Digital Multimeter (DMM) combines the advantages of a compact and versatile multimeter with the precision and convenience of a digital instrument. Automatic range selection and polarity decision give rapid readings. The complete absence of range switching enables the user to concentrate on the task in hand and apart from selecting the actual measurement mode required all other measurement decisions are undertaken automatically, so reducing the risk of damage to the user's equipment, as well as to the DMM.

The DMM covers the following measurement modes, all auto-ranging.

DC VOLTAGE

10μV - 1000V

AC VOLTAGE

10μV - 750V

RESISTANCE

100mΩ - 11MΩ

DC CURRENT

1nA - 1.1mA

With a scale length of 109.999.

Model 7050 also incorporates an automatic over-range indication, automatic overload protection and automatic blanking of unused digits.

Model 7054 incorporates a digital output in parallel BCD form for use with printers and other output devices.

SECTION 2 Operation

This section provides all the necessary instructions concerning preliminary adjustments and operating procedures required to put the instrument into everyday use.

PRELIMINARY ADJUSTMENTS

Before using the instrument for the first time the following preliminary adjustments should be carried out:

(a) Check that the voltage selection switch on the rear panel is in the correct position.

(b) Check that the correct fuse is fitted as follows:-

230V	150mA	Slo-Blo	1¼" x ¼"
115V	300mA	Slo-Blo	1¼" x ¼"

(c) Connect a suitable connector to the input mains lead as follows:-

Brown	-	Line (Live)
Blue	-	Neutral
Yellow/Green	-	Earth

(d) Plug into the mains supply and switch the instrument ON.

OPERATION

The operation of this instrument under most conditions will be found to be self-evident. The only operator decision required is the selection of the measurement mode required.

During operation, the following factors should be borne in mind:-

1. Since the instrument will automatically change ranges to suit the applied input potential, care should be taken to note the decimal point position in combination with the unit indicators.

2. In the event of an unintentional voltage or current overload, the offending potential should be removed as soon as possible since continuous overload may eventually cause damage to the instrument.

3. Due to the high input impedance of the input amplifier, the display readings will be random when the instrument is left with its input terminals as follows:-

   (a) Open circuited on 'V.DC' and 'V.AC' modes.

   (b) Short circuited on 'μA' mode.

   Random readings can cause the range relay to switch on and off which can be prevented by short circuiting the input terminals in the case of (a) and open circuiting them in the case of (b).

4. In the 'Ω' mode, open circuited input terminals produce an overload condition i.e. a steady '1' being displayed. Short circuited input terminals produce a nominal zero condition.

5. When measuring voltages on the lowest range and resistance on the highest range of the DMM, pick-up on the input leads may become a problem. If this occurs it is recommended that the leads be kept as short as possible and/or screened.

SECTION 3 Servicing

This section provides detailed servicing information for the instrument. Setting-up procedures and calibration are covered in Section 4.

INTRODUCTION

This Servicing Section is based on the functional block system of circuit diagrams, whereby components are grouped together to form a functional entity. A large scale block diagram is used to describe the overall operation of the Digital Multimeter (DMM). This diagram is then sub-divided to produce blocked circuit diagrams.

Information regarding circuit descriptions, component locations, printed circuit board layouts and any specific cautionary notes concerning components or testing procedures are arranged to be fully visible with the appropriate circuit diagram. Full calibration and setting up procedures are located in Section 4.

PRESENTATION OF INFORMATION

A brief glance through this section will reveal that the section is sub-divided into three major sub-sections, each of which deals with a major function in the DMM. Located within each section are block type circuit diagrams, always folding out clear to the right, with a functional description of each on the left hand text page. The pcb layout diagrams are arranged to fold out clear to the left, allowing cross reference between diagram and component location.

Referring to any of these diagrams, it can be seen that the major functional signal pathways are shown as bold lines, whilst those of a minor or control function are shown with thinner lines. The arrows indicate the direction of functional flow, which in the majority of cases will be from left to right of the diagram. Most feedback paths however, will flow from right to left.

These rules, although generally followed, are not rigidly adhered to where observance may cause ambiguity or is extravagant of space.

COMPONENT LOCATION

Diagrams of the printed circuit boards associated with each circuit diagram and photographs illustrating the method of access are reproduced in a manner enabling them to be examined in conjunction with the diagrams. By this method the physical position of any component can be quickly established.

COMPONENT NUMBERING

Each printed circuit has its own component numbering. This means that on a circuit diagram more than one component may be shown with the same component number. When this occurs care must be taken to ensure that the correct part is identified if it is required to replace the component. For instance, in the 7050 there are several pcb's, all of which include a component numbered R1.

The correct item must be identified from the parts list by reference to the pcb or assembly on which it is mounted.

POWER RAIL NOTATION

The power rails are shown as short detached bars with the nominal voltage annotated. On any one pcb, all bars annotated with the same voltage are electrically connected together and correspond to the appropriate rail notation shown on the power supplies circuit diagram, referenced 10.

The 0V rail in some cases is associated with the signal paths, annotated SIGNAL 0V and followed by a reference number 1 to 4 inclusive, thereby identifying the decoupling components used for that particular group of components. All identically referenced zero volt lines are electrically connected together at the 0V STAR POINT on pcb 1 (C18 –ve).

It must be remembered that the voltages shown are approximate, being proportional to the load taken through the appropriate decoupling resistors. A voltage reading which is inconsistant with the value given on the diagram should not, therefore, be taken as a symptom of unserviceability without reference to other indications.

ELECTRICAL CONNECTIONS

Electrical connections used are mainly of the Berg pin and socket type. Two plugs and sockets are employed using Berg pin/socket combinations. These are clearly identified, with all the remaining Berg pin/socket connections bearing only a number.

Transformer connections used are of the disconnect pin type.

SPLIT PADS

The split pads provide a means of adjusting circuit resistance and also for isolating various parts of the circuit during fault diagnosis.

They are short circuited by running solder across the gap and open circuited by removing the solder track. Care should be taken not to apply excessive heat during these operations.

FUNCTIONAL DESCRIPTION

The Model 7050 Digital Multimeter (DMM) may be looked upon as an instrument which divides down into three major functional areas. These are shown as coloured areas in the adjacent KEY DIAGRAM.

This diagram should be looked upon as a pictorial index as within each of these coloured areas are further blocks, each referenced with a number which refers to a specific block/circuit diagram within each section of this manual.

It is important when using these diagrams that the information should be looked at from a functional view-point before dealing with any actual detailed servicing. That is to say, deduce what could be the problem before actually looking at specific circuit details.

With reference to the KEY DIAGRAM, the input signal is applied to an ANALOGUE signal processing section. The primary function of this block is to scale the input signal into a form suitable for use by the DIGITAL (A/D Converter) section.

The input signal in all cases is converted into a dc signal. Since the A/D Converter can only handle signals within the range 0-11V directly, the analogue section provides a 100/1 attenuation on the higher ranges, also 10/1 on the acV mode.

The scaled analogue input is then converted into a digital form by means of the triple ramp technique of integration (for a detailed explanation, refer to Section 3B), the result of which is displayed on a light emitting diode (LED) display.

The third major functional block provides the power supplies to operate the whole instrument. This block also provides timing pulses to relate the measurement to the incoming mains supply frequency in order to overcome ac interference.

GENERAL NOTE:-

The numbers in each of the blocks shown below refer to the appropriate block and circuit diagrams contained in this section.

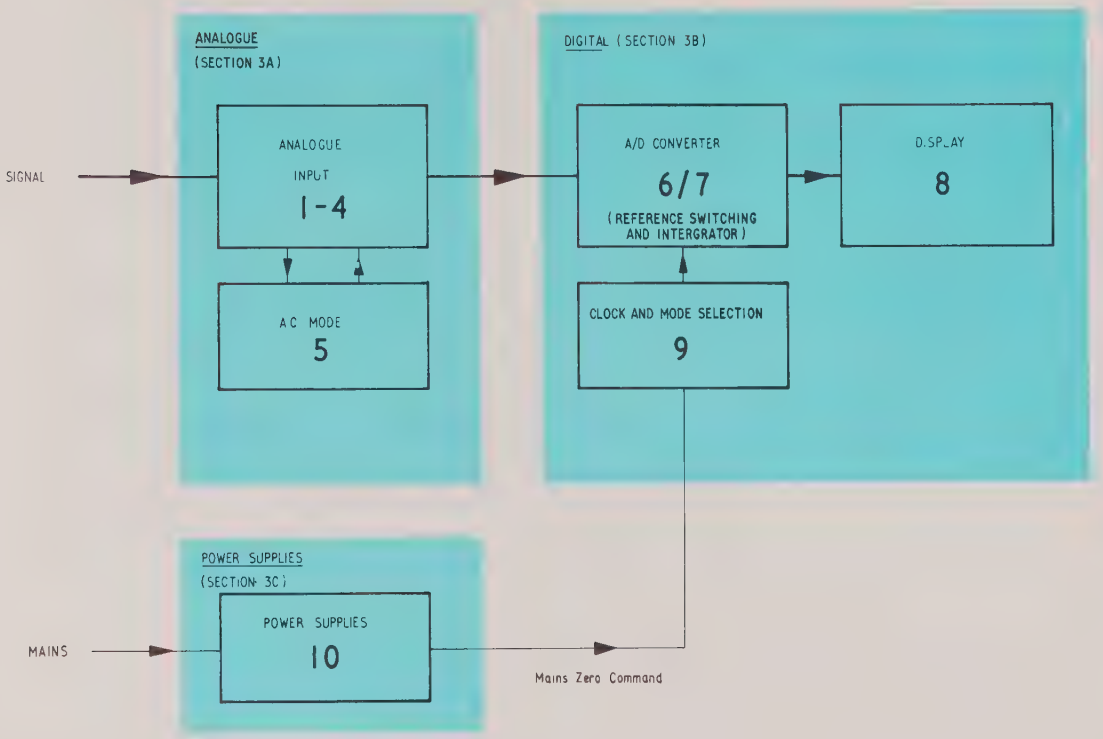


Fig. 3.1. Key Diagram (Pictorial Index).

This sub-section deals with the ANALOGUE section of the instrument whose primary function is to convert the input signal into an acceptable form suitable for digital conversion by the DIGITAL section (SUB-SECTION 3B - DIGITAL).

SIGNAL CONVERSION

INTRODUCTION

The purpose of these sections of circuitry is to convert the incoming signal into dc suitable for conversion by the A/D Converter in the DIGITAL section of the instrument.

DC MEASUREMENT

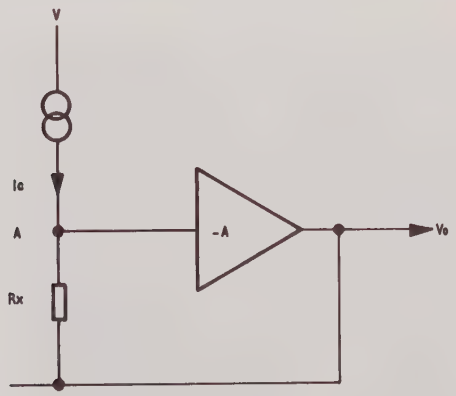
In this mode of operation, since the applied signal is already dc, the circuitry serves to scale the input to within the upper 11V limit acceptable to the A/D Converter input.

The INPUT AMPLIFIER is arranged in a series feedback configuration to provide a very high input impedance to the applied signal on the unattenuated ranges (0-11V).

The Analogue Input circuit in the 'V.DC' mode is shown on DIAGRAM 1.

RESISTANCE MEASUREMENT

The resistance measuring mode, 'Ω', is shown on DIAGRAM 2. Consider the following simplified diagram.



Point A is a 'virtual earth' input to a very high gain amplifier (INPUT AMPLIFIER). In order that the current flowing into and out of point A is balanced, the output of the amplifier Vo must rise to develope a potential drop across the applied unknown resistance Rx such that the constant current Ic derived from the reference voltage all flows through Rx. The final value of Vo when the circuit balances will be proportional to Rx and it is this output which is used by the A/D Converter for conversion to units of resistance.

CURRENT MEASUREMENT

Following from the above description of resistance measurement, it can be seen that if we make Rx a known value (RV6/R6 on DIAGRAM 3), the output of the amplifier Vo will be proportional to the unknown applied current.

AC MEASUREMENT

The section of circuitry used for converting the applied input to dc is shown separately on DIAGRAM 5.

The applied signal passes through a separate INPUT ATTENUATOR network and, via the AC AMPLIFIER buffer stage and SCALING RESISTORS, to the SUMMING JUNCTION. This point acts as a 'virtual earth' to the INPUT AMPLIFIER which follows. The output of this amplifier passes through the RECTIFIER SYSTEM which then divides the amplifier output into positive and negative half cycles by rectifier action. The positive half cycle output is filtered by the LOW PASS FILTER to form the equivalent dc input to the A/D Converter.

Since the rectified output would produce the mean value of the applied input, provision is made (RV3) to scale the signal input such that the final displayed reading is the rms (root mean square) as opposed to mean value of the applied signal. It should be remembered that this scaling action will only be valid when the input wave form is sinusoidal.

TEST WAVEFORMS

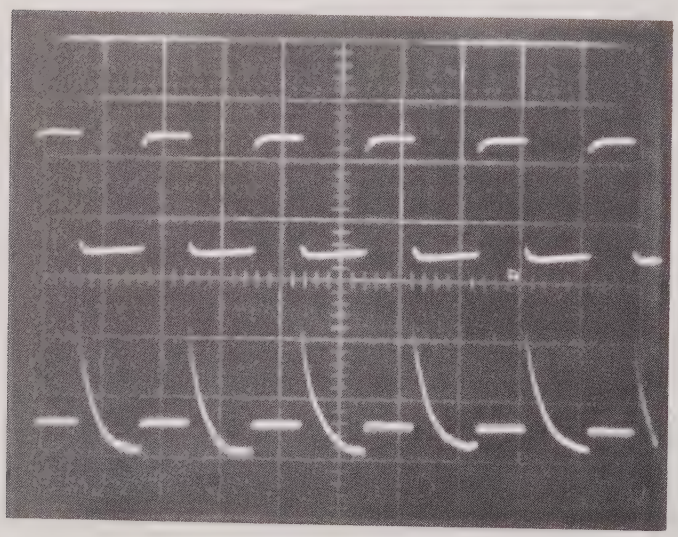
FRAME 3A - 1

UPPER TRACE

A typical output waveform produced by the CHOPPER DRIVE (DIAGRAM 4) at TR4 collector. The output at TR3 collector is an inverted form of this trace.

LOWER TRACE

A typical output waveform produced by the DEMODULATOR (DIAGRAM 4) at the junction of C5 and R11.



Time/cm:- 2ms.

Volts/cm:- 500mV.

Frame 3A-1 Chopper/Demodulator waveforms.

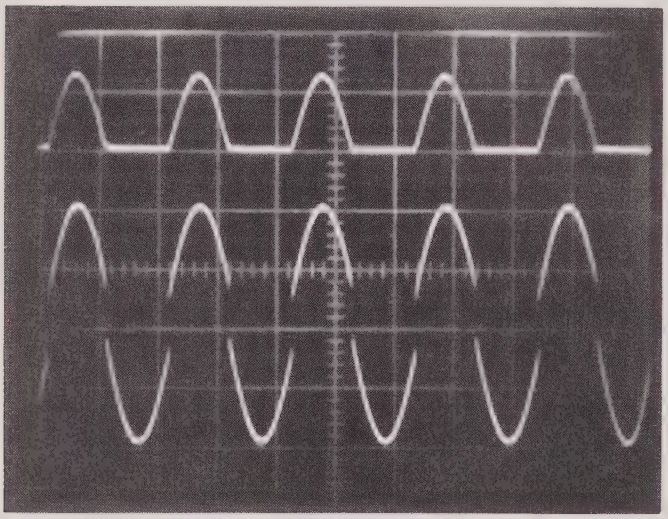
FRAME 3A - 2

UPPER TRACE

A typical output waveform produced at diode D3 cathode, the output from block RECTIFIER SYSTEM (DIAGRAM 5) used to provide dc to the A/D Converter for operation on ac V mode.

LOWER TRACE

A typical output waveform provided by the complementary common base stage formed by TR1/2 in block RECTIFIER SYSTEM (DIAGRAM 5) and used to drive both halves of the diode feedback loop. The sharp transitions about the zero of the output waveform overcome possible non-linear rectification, due to diode characteristics up to about 0.7V.



Time/cm:- 1ms.

Volts/cm:- 1V.

Frame 3A-2 Rectifier System waveforms.

DC MODE

In this mode of operation the correct attenuation is applied by the Auto Ranging function of the instrument.

DC ATTENUATOR/RESISTOR

The attenuation available on 'V.DC' is decided by relay RLB as follows:-

RLB energised:- 100/1 attenuation

RLB de-energised:- no attenuation

INPUT AMPLIFIER

This acts as a buffer between the voltmeter input and the Integrator (DIAGRAM 7).

OHMS MODE

In this mode of operation, the −10.000V output from the Inverter (REFERENCE SWITCHING, DIAGRAM 6) is used to provide a constant potential which, in conjunction with the DC Attenuator/ Resistor, produces the appropriate test current (100μA or 1μA). The test current whilst flowing through the unknown resistance, produces a potential drop which is proportional to the value of unknown resistance. Refer to diagram 6 for further details of the −10.000V voltage source.

DC ATTENUATOR/RESISTOR

This resistance network is normally used as the DC Attenuator. When the 'Ω' mode is selected the network, in conjunction with relay RLB, decides the value of test current as follows:-

RLB energised:- 1μA nominal

RLB de-energised:- 100μA nominal

INPUT AMPLIFIER

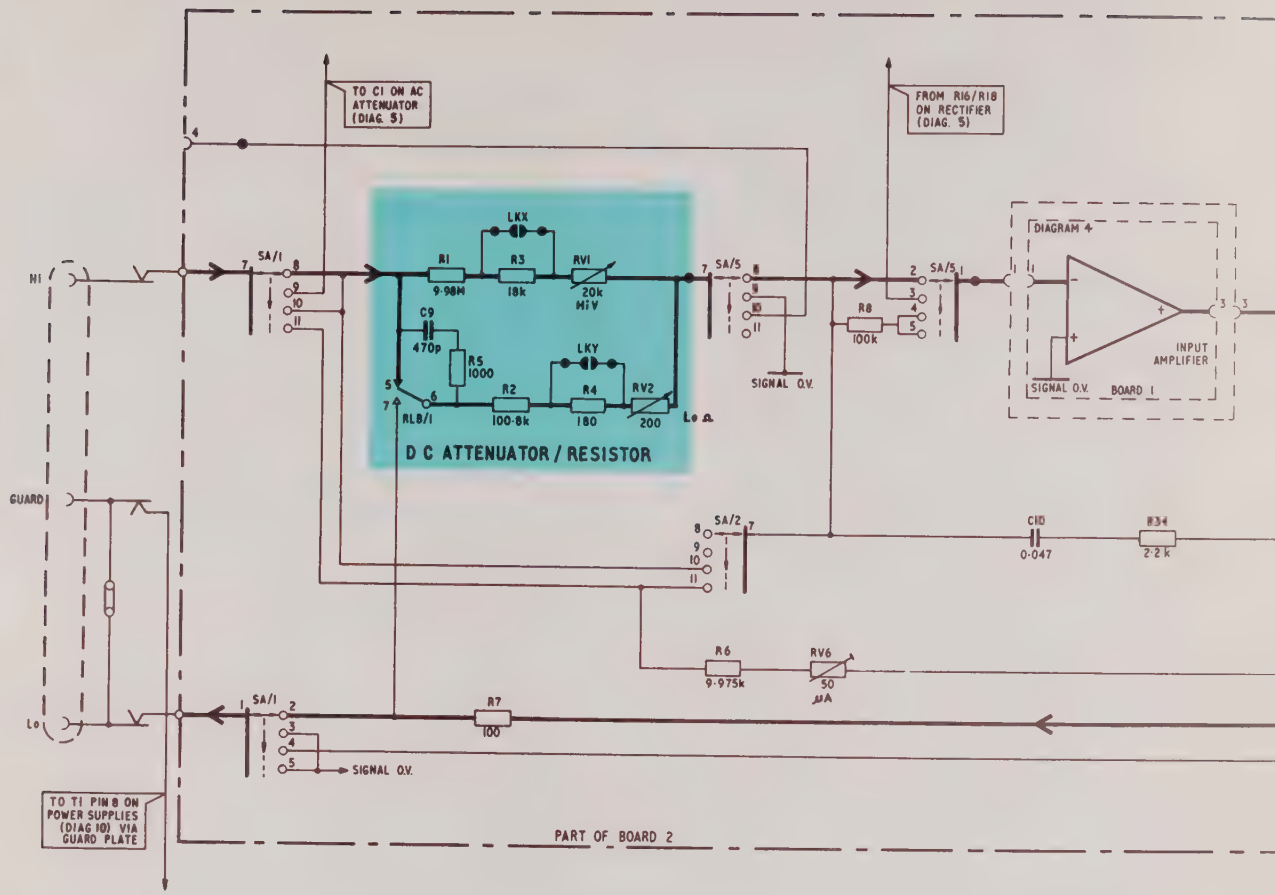
This is used in operational amplifier configuration with the unknown resistor as the feedback resistor.

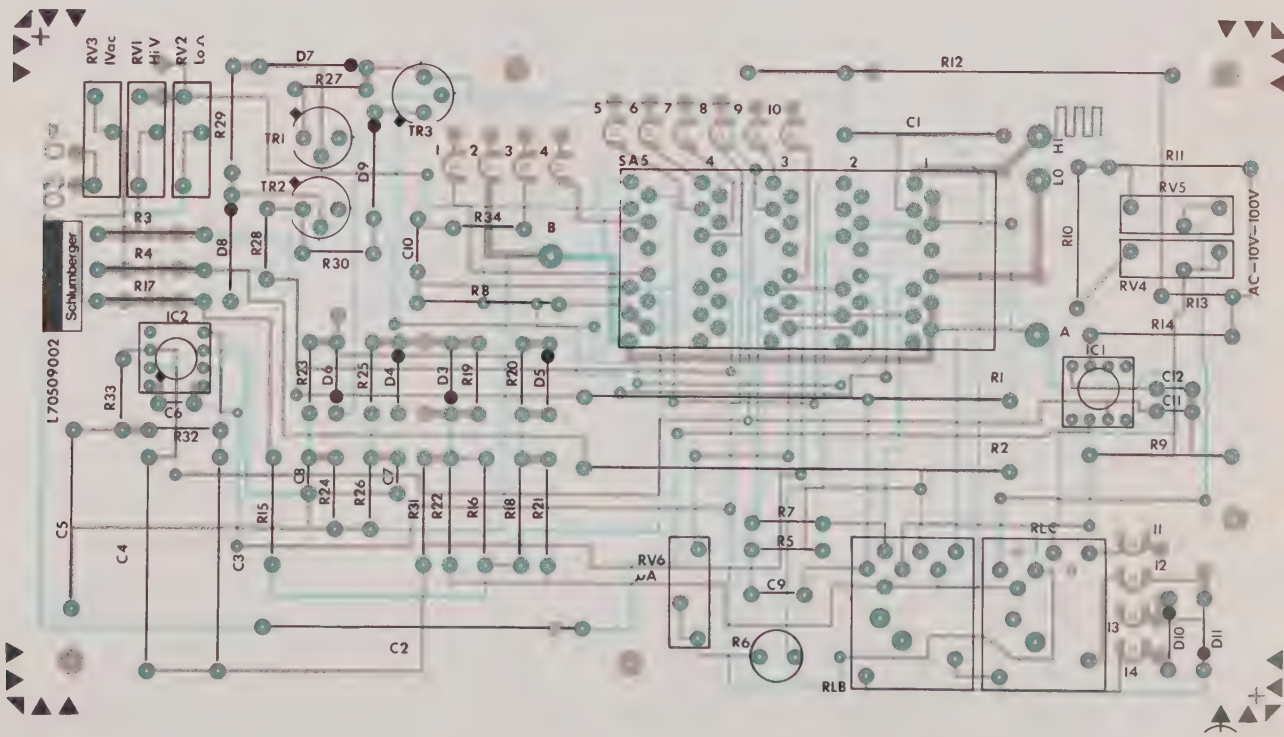
CURRENT MODE

In this mode of operation the unknown current flows through a known resistance R6, thereby producing a potential drop across it which is proportional to the unknown current.

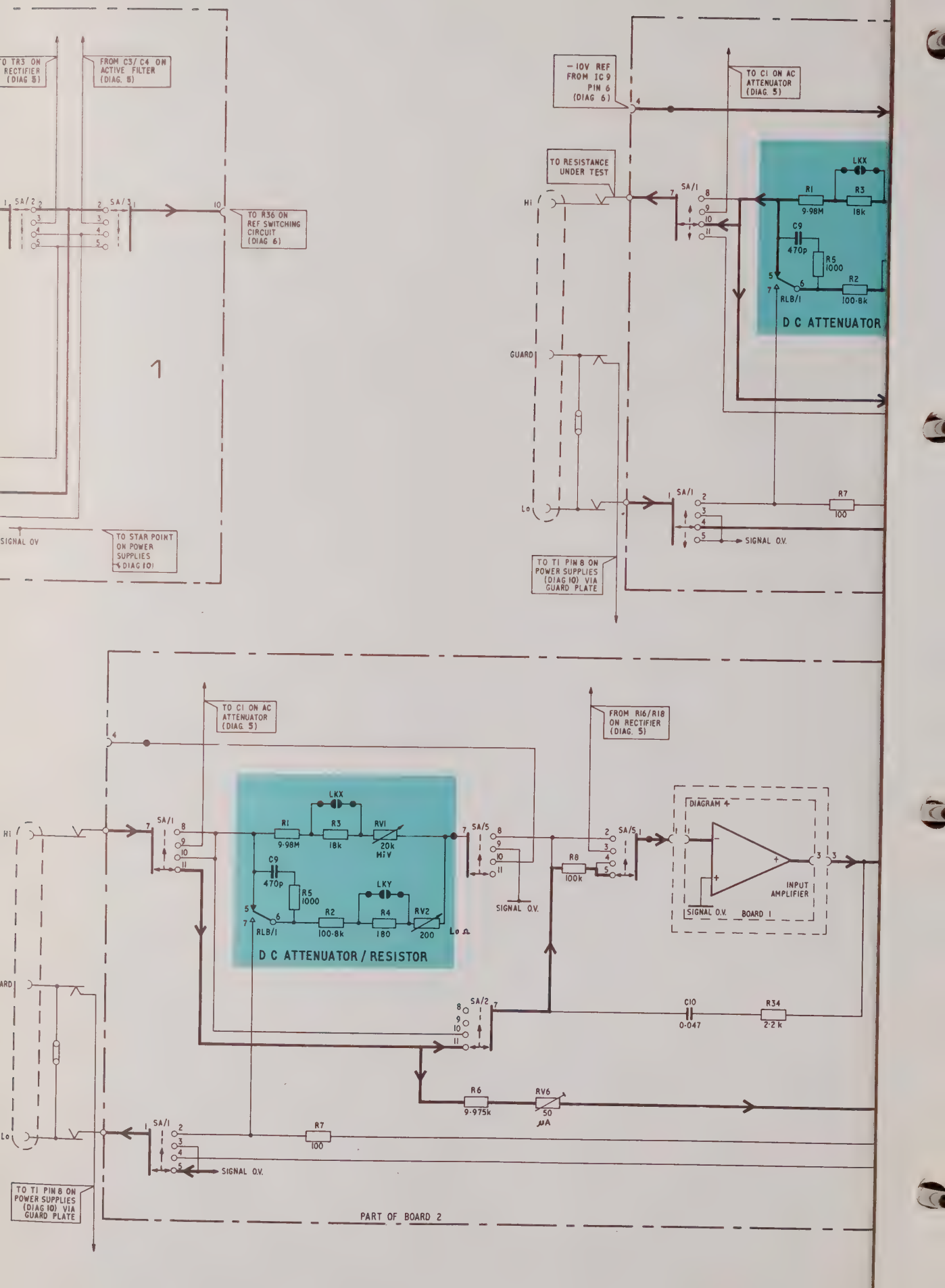
INPUT AMPLIFIER

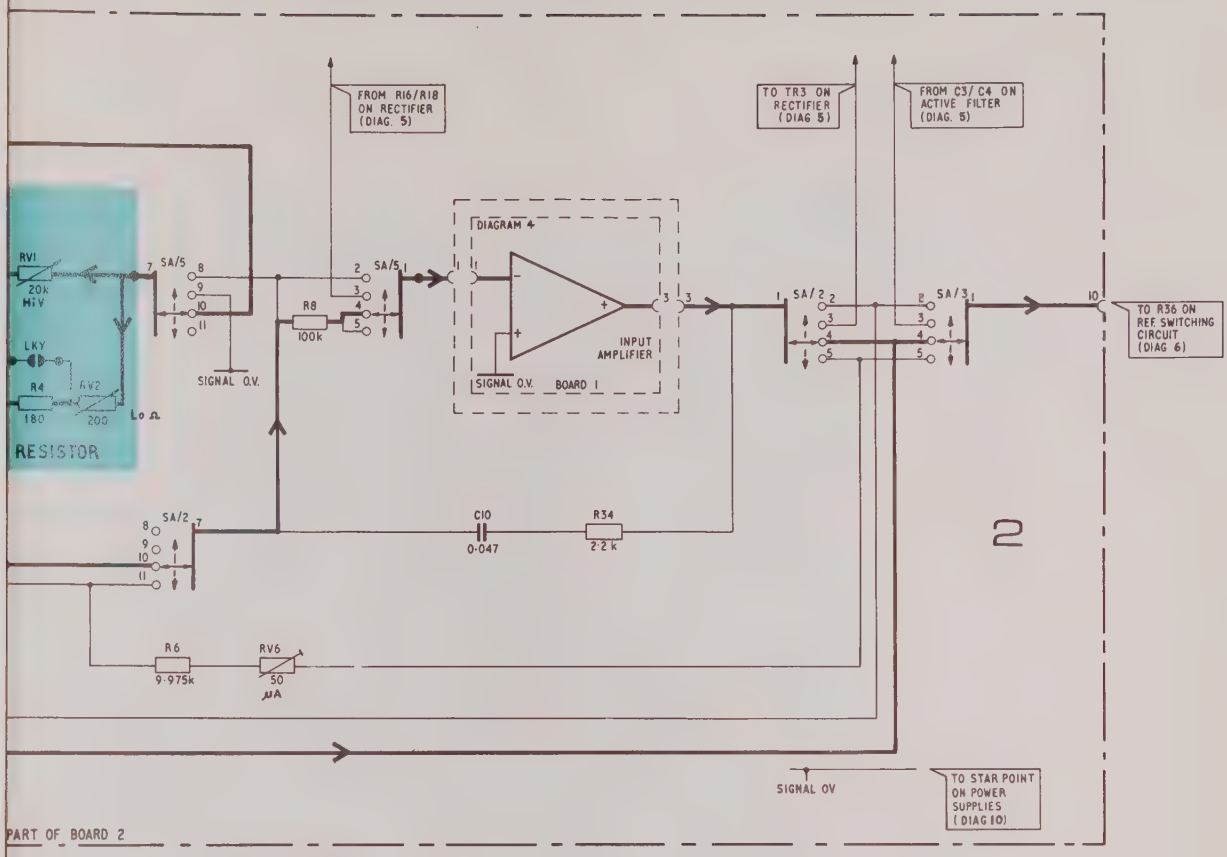
This is used in operational amplifier configuration with the unknown current fed to the virtual earth.


TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG. 5)
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V. BOARD 1
HI
LO
GUARD
SA/1
SA/2
SA/5
LKX
LKY
R1 9·98M
R3 18k
RV1 20k HiV
C9 470p
R5 1000
R2 100·8k
R4 180
RV2 200
RLB/1
Lo Ω
D C ATTENUATOR / RESISTOR
R8 100k
SIGNAL O.V.
C10 0·047
R34 2·2k
R6 9·975k
RV6 50 μA
R7 100
SIGNAL O.V.
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
PART OF BOARD 2

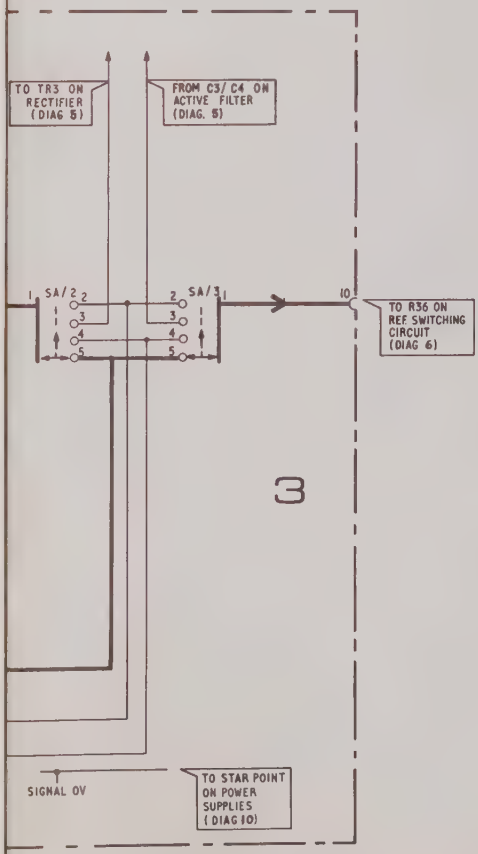

RV3 IVac
RV1 HiV
RV2 Lo Ω
Schlumberger
L70509002
SA5
AC—10V—100V
RV5
RV4
IC1
IC2
RLB
RLC
RV6 μA

2a


TO TR3 ON RECTIFIER (DIAG 5)
FROM C3/ C4 ON ACTIVE FILTER (DIAG. 5)
SA/2
SA/3
TO R36 ON REF SWITCHING CIRCUIT (DIAG 6)
SIGNAL OV
TO STAR POINT ON POWER SUPPLIES (DIAG 10)
-10V REF FROM IC 9 PIN 6 (DIAG 6)
TO C1 ON AC ATTENUATOR (DIAG 5)
TO RESISTANCE UNDER TEST
Hi
SA/1
LKX
R1
9·98M
R3
18k
C9
470p
R5
1000
R2
100·8k
RLB/1
D C ATTENUATOR
GUARD
Lo
R7
100
SIGNAL O.V.
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
TO C1 ON AC ATTENUATOR (DIAG. 5)
FROM R16/R18 ON RECTIFIER (DIAG. 5)
RV1
20k
Hi V
SA/5
R8
100k
DIAGRAM 4
INPUT AMPLIFIER
SIGNAL O.V.
BOARD 1
LKY
R4
180
RV2
200
Lo Ω
D C ATTENUATOR / RESISTOR
SA/2
C10
0·047
R34
2·2 k
R6
9·975k
RV6
50
μA
TO T1 PIN 8 ON POWER SUPPLIES (DIAG 10) VIA GUARD PLATE
PART OF BOARD 2



NOTE :- TEST CURRENT
RLB/1 CONTACTS 5-6 FOR 100μA
RLB/1 CONTACTS 7-6 FOR 1μA


TO TR3 ON RECTIFIER (DIAG 5)
FROM C3/ C4 ON ACTIVE FILTER (DIAG. 5)
SA/2
SA/3
TO R36 ON REF. SWITCHING CIRCUIT (DIAG 6)
3
SIGNAL OV
TO STAR POINT ON POWER SUPPLIES (DIAG 10)

1 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN DC MODE)*

2 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN OHMS MODE)*

2a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*

3 *ANALOGUE INPUT CIRCUIT DIAGRAM (IN CURRENT MODE)*

INPUT AMPLIFIER

PROTECTION NETWORK

D1 and D2 protect the CHOPPER AMPLIFIER during overload conditions. D3/D4 in conjunction with D5/D6 limits the OUTPUT AMPLIFIER output to within ± 12V.

LOW-PASS FILTER

R3, R4 and C1 form a low-pass filter which removes the high frequency components (> 100Hz) from the dc channel and prevents spikes from the CHOPPER (Modulator) circuitry reaching the input terminals.

CHOPPER DRIVE

A 275Hz emitter-coupled Multivibrator TR3/4 for driving the CHOPPER and DEMODULATOR.

A small proportion of the anti-phase output is applied via RV2 to minimise chopper-spikes produced by TR1 in the CHOPPER (Modulator) circuitry.

(Refer to Section 4 - Setting Up Procedure for details on the adjustment of RV2).

CHOPPER (MODULATOR)

The filtered output from the LOW PASS FILTER is 'chopped up' by alternately shorting the signal to earth via TR1 to form an ac type signal. The chopping frequency is determined by the in-phase output of the CHOPPER DRIVE multivibrator.

Anti-phase chopper drive is applied to G2 of TR1 to minimise chopper spikes.

RV1 (Vo) provides a small dc voltage to the Chopper output, compensating for small offsets.

CHOPPER AMPLIFIER

IC1, whose gain and frequency response are defined by C3, C4, R8 and R9, amplifies the input (chopped) waveform produced by the CHOPPER (Modulator). The ac gain is 10,000 and the dc gain is unity.

DEMODULATOR

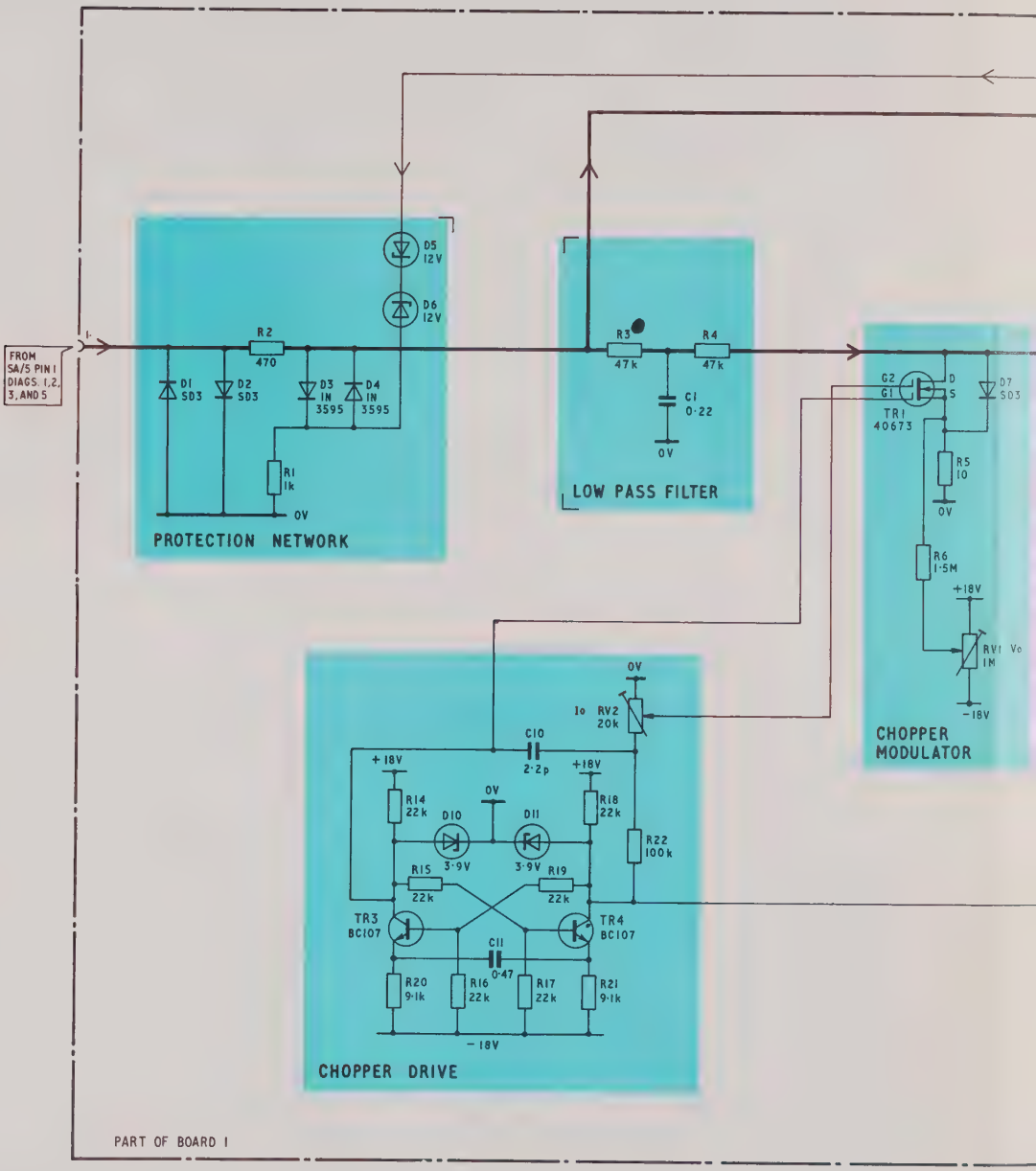
The output from the CHOPPER AMPLIFIER is fed via C5 to TR2 where it is dc restored. The ac component is removed by filter R11 and C6, leaving the dc component only.

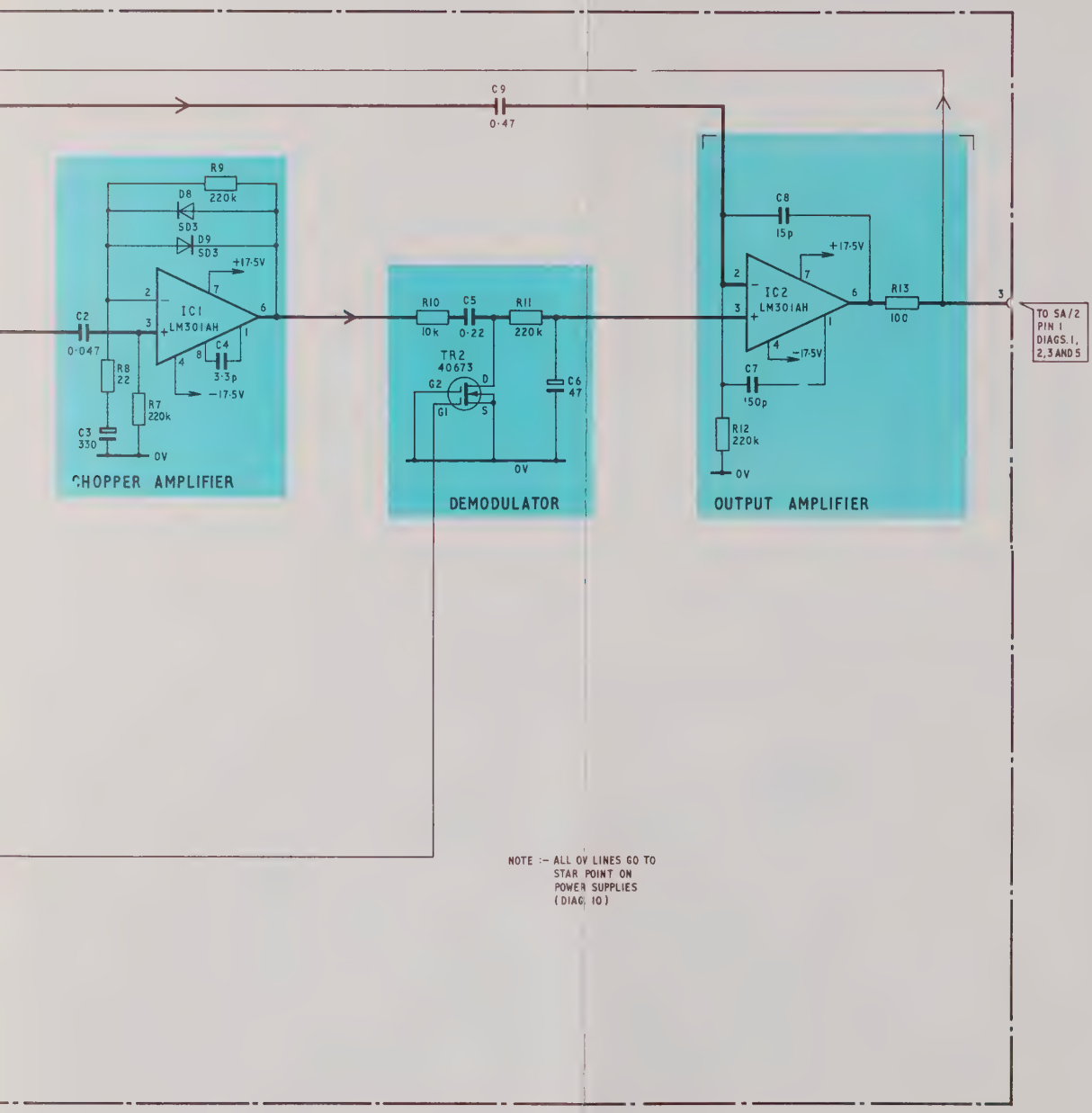
OUTPUT AMPLIFIER

The ac component (> 2Hz) of the input voltage is coupled directly via R12/C9 to the inverting input of the amplifier while the dc component on C6 (DEMODULATOR) is added into the non-inverting input.

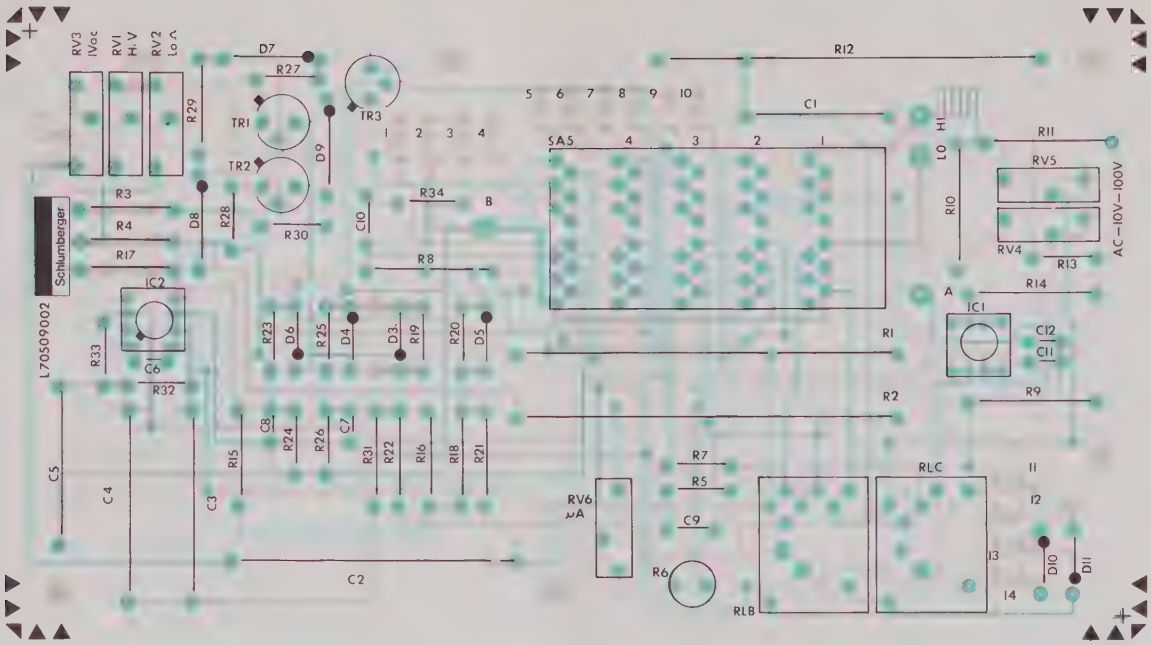
The output is applied to the PROTECTION NETWORK which limits the over-all amplifier output to within ± 12V.

DIAGRAM 3a PCB 1 COMPONENT AND COPPER TRACK LAYOUT

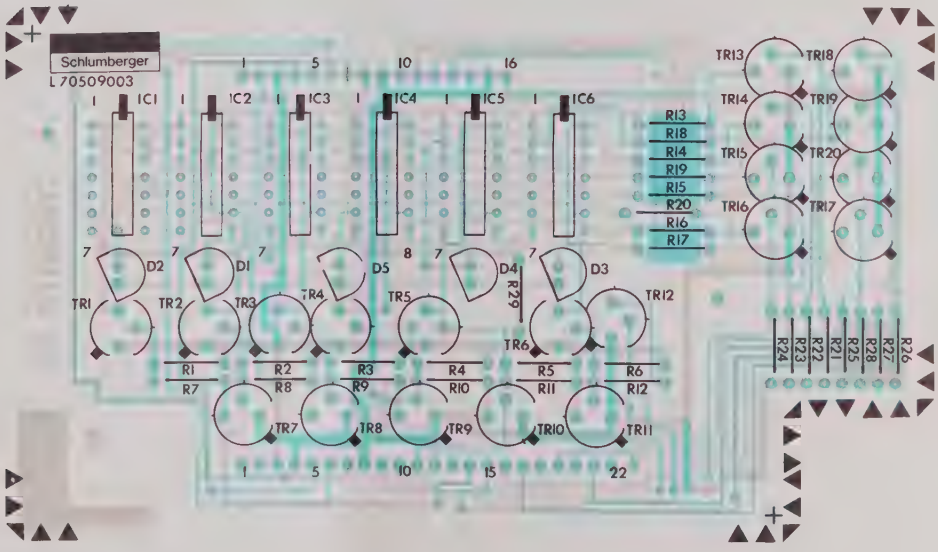

FROM SA/5 PIN 1 DIAGS. 1, 2, 3, AND 5
D5 12V
D6 12V
R2 470
D1 SD3
D2 SD3
D3 IN 3595
D4 IN 3595
R1 1k
0V
PROTECTION NETWORK
R3 47k
R4 47k
C1 0·22
0V
LOW PASS FILTER
G2
G1
D
S
TR1 40673
D7 SD3
R5 10
0V
R6 1·5M
+18V
RV1 1M
Vo
-18V
CHOPPER MODULATOR
0V
Io RV2 20k
C10 2·2p
+18V
+18V
R14 22k
0V
R18 22k
D10
D11
3·9V
3·9V
R22 100k
R15 22k
R19 22k
TR3 BC107
TR4 BC107
C11 0·47
R20 9·1k
R16 22k
R17 22k
R21 9·1k
-18V
CHOPPER DRIVE
PART OF BOARD 1



4 INPUT AMPLIFIER CIRCUIT DIAGRAM



4a *PCB 2 COMPONENT AND COPPER TRACK LAYOUT*



4b *PCB 3 COMPONENT AND COPPER TRACK LAYOUT*

AC MODE

INPUT ATTENUATOR

On the 100V and 750V ranges, relay RLB is energised to attenuate the input signal by a factor of 100. On the 10V range RLB and RLC are energised to attenuate the input signal by a factor of 10. The input impedance is 1MΩ whether the attenuator is energised or not.

AC AMPLIFIER

This is a voltage follower stage, isolating the input from the SCALING RESISTORS. R14 in conjunction with IC1 provides overload protection.

SCALING RESISTORS

The applied input plus the feedback signals via R16/R18 in the RECTIFIER SYSTEM are summed at the 'virtual earth' of the INPUT AMPLIFIER. RV3 scales the input signal so that the final displayed value on the LED module represents the rms (root-mean-square) value of the applied input assuming a pure sine-wave shape.

RECTIFIER SYSTEM

The output of the INPUT AMPLIFIER (DIAGRAM 4) drives the complementary common base stage formed by TR1/2. Positive half-cycles are fed back to the 'virtual earth' via D4/D3 and precision resistor R16. Negative half-cycles are fed back via D6/D5 and R18. Only the positive half-cycles are taken for digital conversion.

R25/R26/C7 and R23/R24/C8 are shaping networks which improve frequency response at low signal levels.

LOW PASS FILTER

IC2 is connected as a low-pass active filter to remove high frequency components from the rectified ac signal. The filter has a nominal cut-off frequency of 3Hz and provides at least 60dB per decade attenuation.

DIAGRAMS 4a & 4b PCB 1 & 2 COMPONENT AND COPPER TRACK LAYOUTS

This sub-section deals with the DIGITAL section of the instrument whose primary function is to convert the dc analogue input into digital form.

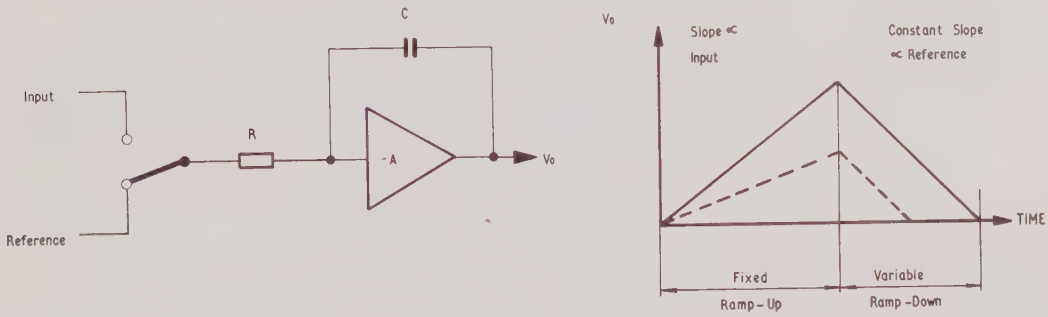
TRIPLE RAMP DIGITAL CONVERSION

INTRODUCTION

The triple ramp technique of analogue to digital conversion may be considered as a refined version of the well known dual ramp technique with the addition of a third ramp. This third ramp (known as fine ramp-down) acts like a 'vernier' upon the usual ramp-down period.

BASIC PRINCIPLES OF OPERATION

Examination of the following simplified cirucit diagram serves to illustrate the principles used to perform analogue to digital conversion in this instrument.



BASIC DUAL-RAMP SYSTEM

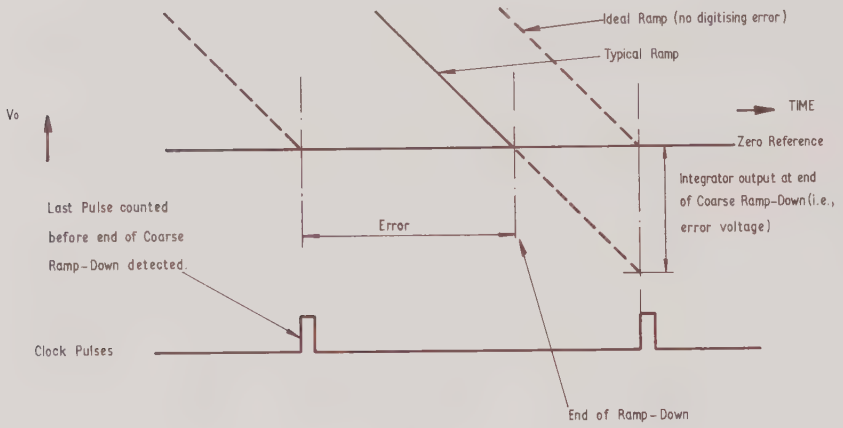
When the integrator is connected to the input its output 'ramps-up' at a rate which is proportional to the value of the input. After a fixed time the switch changes over and connects the reference in place of the input. It is so arranged that the reference voltage is of opposite polarity to that of the input, so that the integrator output now 'ramps-down' at a defined rate which is determined by the value of the reference.

If the ramp-up period is made constant by using a clock pulse generator to gate the input switch, the number of pulses produced during the 'ramp-down' period, the length of which is controlled by the slope of the reference voltage, will be directly proportional to the applied input.

Since both ramp-up and ramp-down periods are related to a common timebase, any variations of clock frequency do not affect the reading.

In the DMM, the reference voltage used during this 'ramp-down' period (known as 'coarse ramp-down') is actually 10V, so each ramp-down pulse with a 'full-house' counter length of 10,000 will represent 1mV. The total number of pulses collected between the end of ramp-up and the point where the integrator output was driven to zero is a direct measure of the applied input voltage to within 1mV.

Looking at a greatly magnified view of the integrator output waveform at the point where the integrator output passed through zero, it can be seen that there is an inherent digitising error within the system, the magnitude of which can be 1mV.



If we allow the integrator output to continue beyond zero until the next clock pulse, the integrator capacitor will be charged to a level representing the difference between 1mV and the true measured input.

By adding two extra less significant decades to the counter, the minimum decade would represent 10μV. If we complement* the counter and then re-organise it such that it counts down to zero when driven by further clock pulses, by changing the ramp-down rate, the final count overall could represent the applied input when the integrator output again passes through zero.

In the DMM, this second ramp-down reference voltage is 100mV so that each new clock pulse will represent 10μV. In order to drive the integrator output to zero, the new ramp-down reference polarity is made opposite to the coarse ramp-down polarity. This third ramp is known as 'fine ramp-down'.

It can be seen that the final measurement could, in theory, be within 10μV of the applied input.

* COMPLEMENTING

The action of complementing a number within a counter can be followed by referring to the following example.

We have a hypothetical counter capable of holding a total count of 100 pulses. If we count say 60 input pulses, still required to 'fill-up' the counter will be 100-60 i.e. 40. It is this number which is defined as the complement of the number 60 in this example.

MEASUREMENT CYCLE DRIVES

INTRODUCTION

All stages of analogue to digital conversion are controlled by IC7-board 1, whose outputs turn on or off appropriate FET switches to select the appropriate sections of circuitry required at each stage of a measurement cycle.

ELECTRICAL ARRANGEMENT

There are eight cycle control drive outputs as follows:-

IC7-pin 11	Drift Correct
pin 12	Earth Clamp
pin 13	Spoiler
pin 14	Neg. Fine Reference
pin 15	Pos. Fine Reference
pin 16	Pos. Coarse Reference
pin 17	Neg. Coarse Reference
pin 18	Input Switch

During a typical measurement cycle, each of these pins will assume the states shown in Table 3B-1. The Pause periods 1-4 are for internal use within the integrated circuit to allow time for internal re-organisation of the counter, range selection and other tidying up operations required. The duration of these periods will change depending upon the range, length of ramp-down, spoiler time etc. so differing pause periods should not be interpreted as indications of faulty operation.

TABLE 3B - 1 CONTROL CYCLE SEQUENCE

L = low $\leqslant$ - 16V H = high $\geqslant$ + 8V

IC7 - Board 1

Period	11	12	13	14	15	16	17	18
Drift Correct	L	L	H	H	H	H	H	L
Pause 1	H	L	H	H	H	H	H	L
Ramp-Up	H	H	H	H	H	H	H	L
Spoiler Period	H	H	L	H	H	H	H	L
Pause 2	H	L	H	H	H	H	H	L
Coarse Ramp	H	L	H	H	H	H*	L*	H
Pause 3	H	L	H	H	H	H	H	L
Fine Ramp	H	L	H	L*	H*	H	H	H
Pause 4	H	L	H	H	H	H	H	L

Levels marked* will be inverted when the applied signal input is negative (with respect to the - terminal on the front panel).

AUTO-RANGING

INTRODUCTION

The DMM is fully auto-ranging for all modes of operation. Range switching is divided into two parts, basic range selection and/or attenuator switching.

RANGE SELECTION

Each of the ranges is coded with a letter, the actual range depicted by each being dependent upon the measurement mode selected (refer Tables 3B - 2 to 4).

The basic ranges are coded A, B and C and progress in decade steps with A the highest. A, B or C followed by the letter R indicates the basic range together with the 100/1 or 10/1 attenuator stage, making a range selection with a full scale reading 100 or 10 times greater than that for the basic range alone.

TABLE 3B-2 VOLTAGE MEASUREMENT CODING

Nominal Range	Range of Voltages Displayed	Range Coding DC	Range Coding AC
1000V	1099.00 to 100.00V	AR	AR
100V	109.999 to 10.000V	BR	BR
10V	10.9999 to 1.0000V	A	CR
1V	1.09999 to 1.00000V 999.99 to 0.00mV	B	B

TABLE 3B - 3 RESISTANCE MEASUREMENT CODING

Nominal Range Ω	Range of Resistance Displayed	Range Coding
10M	10999.9 to 1000.0k	AR
1M	1099.99 to 100.00k	BR
100k	109.999 to 10.000k	A
10k	10.9999 to 1.0000k 999.9 to 0.0Ω	B

TABLE 3B - 4 CURRENT MEASUREMENT CODING

Nominal Range	Range of Current Displayed	Range Coding
1000μA	1099.99 to 100.00μA	A
100μA	109.999 to 0.000μA	B

Ranging up or ranging down occurs just after the fine ramp-down period in the measurement cycle, and unless a range change decision occurs, the range in use will remain constant for the remainder of the cycle.

RANGE-UP SEQUENCE

A range-up decision will occur if the total count at the end of fine ramp-down in the counter equals or exceeds 1.1 times that count which corresponds to the nominal full-scale count for the particular range in use. Take for example the 1V range, a range-up decision occurs if the measured voltage is 1.1 volts or higher, making 1.09999V the highest voltage which will not cause a range-up decision.

RANGE-DOWN SEQUENCE

A range-down decision will occur if the total count in the counter after a measurement falls below 0.1 times that which corresponds to nominal full-scale count except when the particular range in use is the lowest for the mode of operation. In this instance, operation will be maintained on that range for all readings down to zero. Therefore for all but the lowest of a group of ranges 0.10000 times the nominal full-scale value is the lowest reading which will not cause a range-down decision.

RANGE SWITCHING (DIAGRAM 7)

The input signal to the INTEGRATOR may or may not be rescaled by means of changing the effective input resistance. When Range A is selected (i.e. Ranges B/C not turned on) the signal is applied through R41 (1M). When Range B or C is selected, the effective input resistance will be 100k (1M//110k $\simeq$ 100k) thus the integrator input signal will be rescaled by a factor of 10. By this method, the input dynamic range of the INTEGRATOR may be 0 - 11V, or 0 - 1.1V respectively. For inputs above 11V, the attenuator relays RLB and RLC provide the following functions:-

RLB/1:- Provides 100/1 attenuation on dc ranging

RLB/2:- Provides 100/1 attenuation on ac ranging

RLC/1:- Provides 10/1 attenuation on ac ranging (in conjunction with RLB/2)

RLC/2:- In conjunction with C49 and a 100k ohm to Vss (internal resistance in IC7) provides a delay of range change (approximately 2 readings) whilst in AC mode.

SELECTED FET'S TR17 - 20 (PCB No. 1)

Whenever any one of these components is replaced, it is essential that a component with the same colour coding is used or alternatively, replace the whole set.

NOTE. Reference should be made to the selection procedure detailed in the APPENDIX section of this manual.

IC7 - PCB No. 1 (MOS - LS1) INTEGRATED CIRCUIT

This 40 - lead dual-in-line ceramic package contains the digital circuitry used to control the measurement cycle, count and gate clock pulses, provide signals to drive the LED display and to rescale the Integrator during auto-ranging.

Details of all pin connections and functions are on the Clock and Mode Selection diagram, referenced 9. Where inputs from, and outputs to IC7 occur on other circuits, these are identified by the effected IC7 terminal number shown enclosed in a square.

WARNING

Before attempting to remove this integrated circuit, ensure that all power supplies are switched off.

MOS Integrated Circuits are prone to damage by static charges. It is therefore advisable to ensure that all items likely to come into contact with MOS ICs and/or the circuits in which they are employed are bonded together and are earthed. Affected ICs are notified on their pcbs.

DISPLAY

INTRODUCTION

The type of display used in this instrument is a light emitting diode (LED) 7-bar segment, time-shared type arranged to display 6 digits and a polarity sign.

7-bar SEGMENT FORMAT

Each of the possible digits, 0 to 9, is displayed using the universally accepted 7-bar segment format. In order to display a digit, a specific group of bars, each comprising a light emitting diode, is energised.

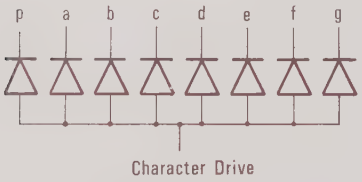
Each bar has been referenced with a letter a-g, and are arranged in the form of a figure 8 as shown below.

For example, suppose we wish to display the digit 2. In this case, bars a, b, d, e and g would be energised, all other bars being left de-energised.

The actual bars used to represent each digit are shown on DIAGRAM 8.

GENERAL ORGANISATION OF DISPLAY

The display used can display up to 6 characters, each of which comprises a 'diode tree' as shown below. The most significant digit can only display a one or a minus.



Each diode of a 'tree' corresponds to a specific bar as detailed above.

NOTE: The decimal point for each character is positioned to the left and will be energised whenever the 'p' bar is called for at the same time as the appropriate character.

In the DMM, each of the 6 possible characters is energised via the appropriate CHARACTER DRIVER (DIAGRAM 8) in sequence. In order that a particular digit may be displayed, the appropriate 7-BAR SEGMENT DRIVERS (DIAGRAM 8) are energised. For a group of diodes to light, both the segment and character drives must be present at the same time but since only one character drive will be present at any one time only one character will ever be on. It should be noted that the 1st character is incomplete, the surplus segments of which are arranged as the UNITS ANNUNCIATOR DISPLAY (DIAGRAM 8).

The polarity window will only display a negative sign, absence of display signifying a positive potential applied to the instrument. When 'V.AC' or 'Ω' is selected, no sign is displayed.

LOGIC ELEMENTS

NAND GATES (DIAGRAM 9)

Elements IC10a and b are logic elements performing a NAND function (positive logic) for which the following truth tables apply:

IC10a Pin No.	1	2	3
	H	H	L
	L	H	H
	H	L	H
	L	L	H
IC10b Pin No.	**4**	**5**	**6**
	H	H	L
	L	H	H
	H	L	H
	L	L	H

Logic Levels

H = -11V to - 14.5V

L = -16.5V to - 17.5V

D - TYPE BISTABLE (DIAGRAM 9)

Elements IC11 a and b are logic bistables (Flip-flops) performing a D-type function (positive logic) for which the following rules apply:

1. Whenever the CK (Clock) input goes high (positive logic), the Q output assumes the same state as that present on the D input.

2. Whenever the CK input is low, the D input level has no effect.

3. The $\overline{Q}$ output is always the complement of the Q output.

VOLTAGE LEVELS

Care should be taken when investigating this section of circuitry not to short any of the logic element connections to the 0V rails, since this action could apply a minimum level of -12V to the element and almost certainly damage it. It is recommended that the -17V rail should be used as a return path for test equipment and make appropriate adjustments to indicated readings.

TEST WAVEFORMS

FRAMES 3B-1/2

UPPER TRACE

This shows a typical input waveform at the INTEGRATOR (DIAGRAM 7) 'virtual earth' input.

LOWER TRACE

A typical ramp-up waveform produced at the input of the X1000 AMPLIFIER (DIAGRAM 7) at C21/R46. The small insert shows a typical fine ramp-down. Note that the coarse ramp-down cycle is shorter than that shown in the main trace for illustration purposes only.

FRAMES 3B - 3/4

UPPER TRACES

These traces illustrate typical CHARACTER DRIVER (DIAGRAM 8) outputs. The outputs are taken from the collector of TR9 instead of the 'floating' collector of TR3, providing a well defined pulse.

LOWER TRACES

These traces illustrate typical 7-BAR SEGMENT DRIVER (DIAGRAM 8) outputs. The outputs are taken from the 'a' bar output, the collector of TR13, and are as follows.

Trace 3B-3 shows the 'a' bar segment, aligned underneath the 3rd character driver output, in a de-energised state. This depicts the missing 'a' bar of the figure 4 in this example.

Trace 3B-4 shows the 'a' bar segment in the energised state, in this example the top of the figure 3.

NOTE:- The traces 3B-3/4 were taken with the BCD Output Module, and its inherent pull-up effect on the SEGMENT DRIVERS, fitted. Under this condition the trace of any bar not selected is pulled up. If tested without this pull-up effect, the position of the non-selected bar trace is indeterminate.

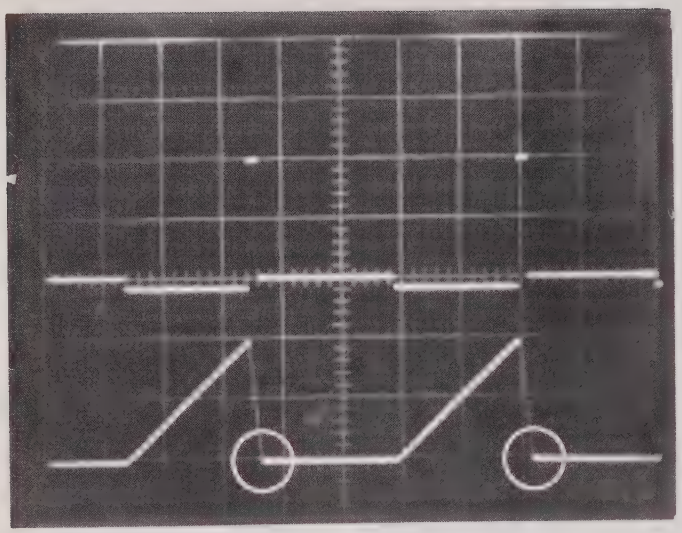
FRAME 3B-5

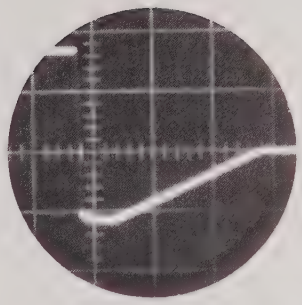
UPPER TRACE

Typical output waveform at IC7-pin 19 of clock input phase ϕ 1 - refer CLOCK DRIVERS (DIAGRAM 9).

LOWER TRACE

This is the clock input at IC7-pin 20 in phase ϕ 2.

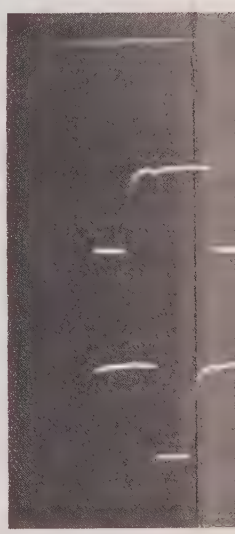




Time/cm:- 50ms.

Volts/cm:- 5V.

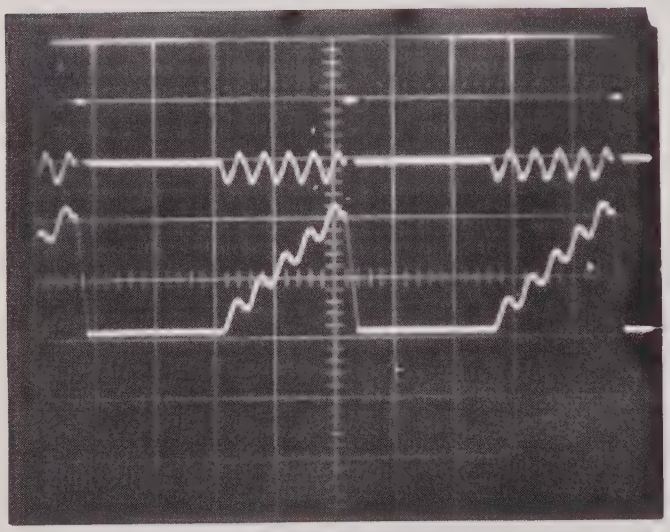
Frame 3B-1 Typical Integrator waveforms.



Time/cm:- 5μs.

Volts/cm:- 20V.

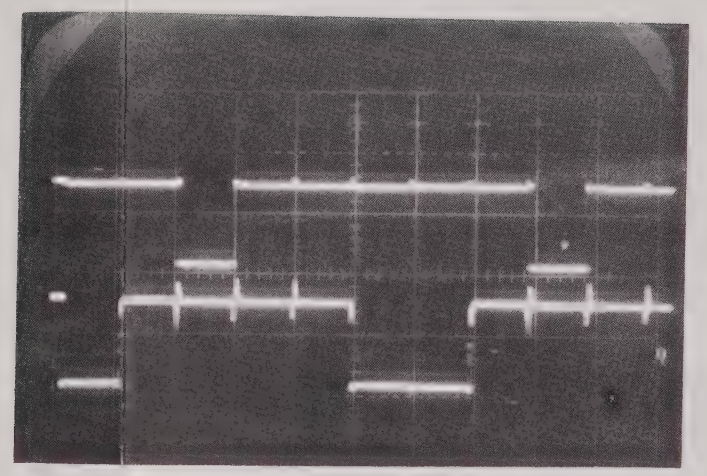
Frame 3B-5 Typical



Time/cm:- 50ms.

Volts/cm:- 10V.

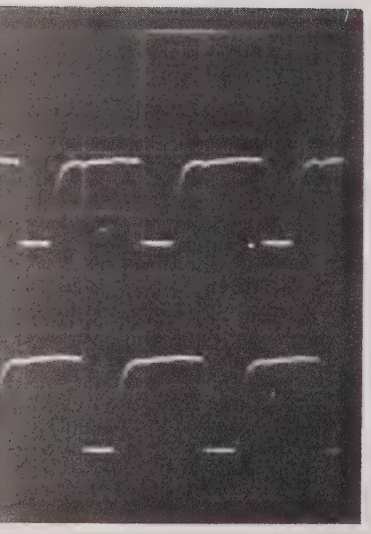
Frame 3B-2 Typical Integrator waveforms with ac interference.



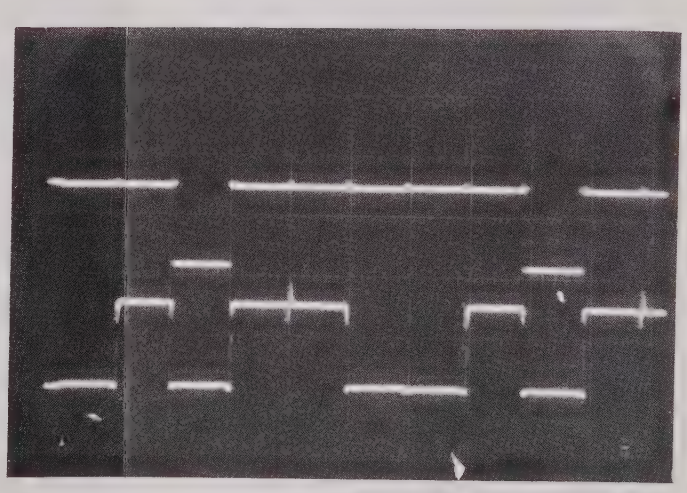
Time/cm:- 200μs.

Volts/cm:- 5V.

Frame 3B-3 3rd Character with 'a' Segment de-energised (e.g. numeral 4).



aveforms.



Time/cm:- 200μs.

Volts/cm:- 5V.

Frame 3B-4 3rd Character with 'a' Segment energised (e.g. numeral 3).

REFERENCE SWITCHING

REFERENCE VOLTAGE SOURCE

IC8 is connected as a non-inverting amplifier amplifying the voltage of reference zener D38 to give + 10V adjusted by means of R97 to 101 and RV7 to give correct calibration. The output is +10.000V for use as a positive coarse reference. R93/R94 form a potential divider to provide + 100mV for use as positive fine reference.

INVERTER

IC9 is connected as an inverter to produce - 10.000V from the REFERENCE VOLTAGE SOURCE. RV8 is adjusted to compensate for resistor tolerance and any dc offset. R104/R105 form a potential divider to provide - 100mV for use as negative fine reference.

EARTH CLAMP

During ramp-up, IC7-pin 12 goes high, thus via TR26 allowing TR15 to conduct to apply the unknown input signal to the A/D Converter. Similarly, TR16 is turned off thus unclamping the INPUT BUFFER AMPLIFIER from signal earth. At the end of ramp-up, IC7-pin 12 goes low, thus turning off TR15 and reclamping the INPUT BUFFER AMPLIFIER to earth via TR16.

INPUT BUFFER AMPLIFIER

A buffer stage providing input isolation to the INTEGRATOR (DIAGRAM 7). RV3 is provided for trimming out any internal voltage offset of IC3 while RV4 adjusts the input current compensation.

INPUT SWITCH DRIVER and INPUT SWITCH

During ramp-up, IC7-pin 18 goes low, applying the unknown input signal to the INTEGRATOR (DIAGRAM 7). TR17 is chosen such that the FET switches TR18 or TR19 in the COARSE REFERENCE SWITCHES and TR17 are of equal impedance to the INTEGRATOR (DIAGRAM 7) during both ramp-up and the appropriate coarse ramp-down period.

(Refer to the FET Selection Procedure in the APPENDIX of this manual for details of selection).

NEG. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a positive input signal during ramp-up, IC7-pin 17 goes low during the coarse ramp-down period. This turns on TR19 applying -10.000V as a negative reference input to discharge the level (proportional to the applied input signal) stored on the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

NEG. FINE REFERENCE SWITCH

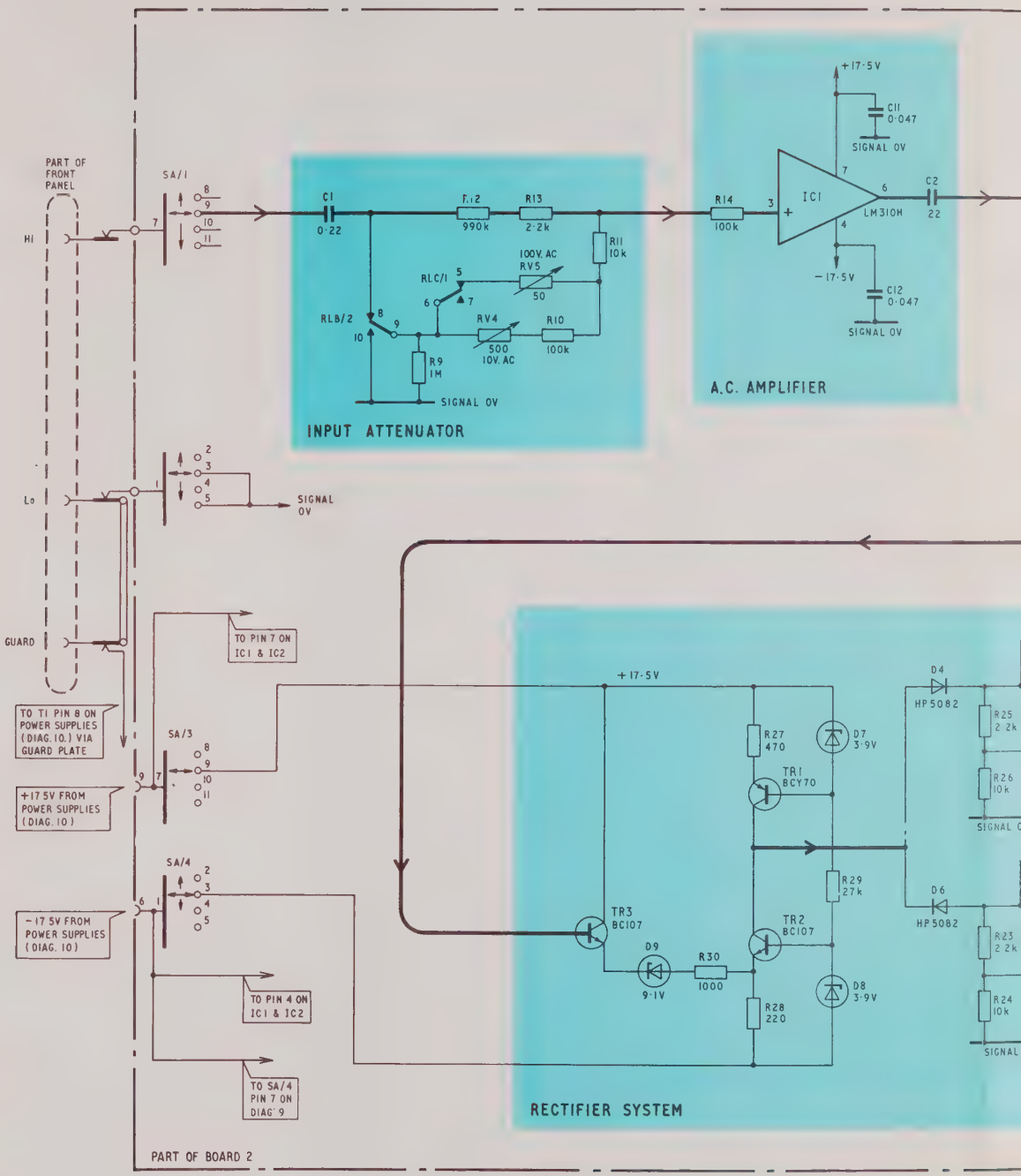
If the input signal was negative during ramp-up, IC7-pin 14 goes low, turning on TR21 during the fine ramp-down period to apply - 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).

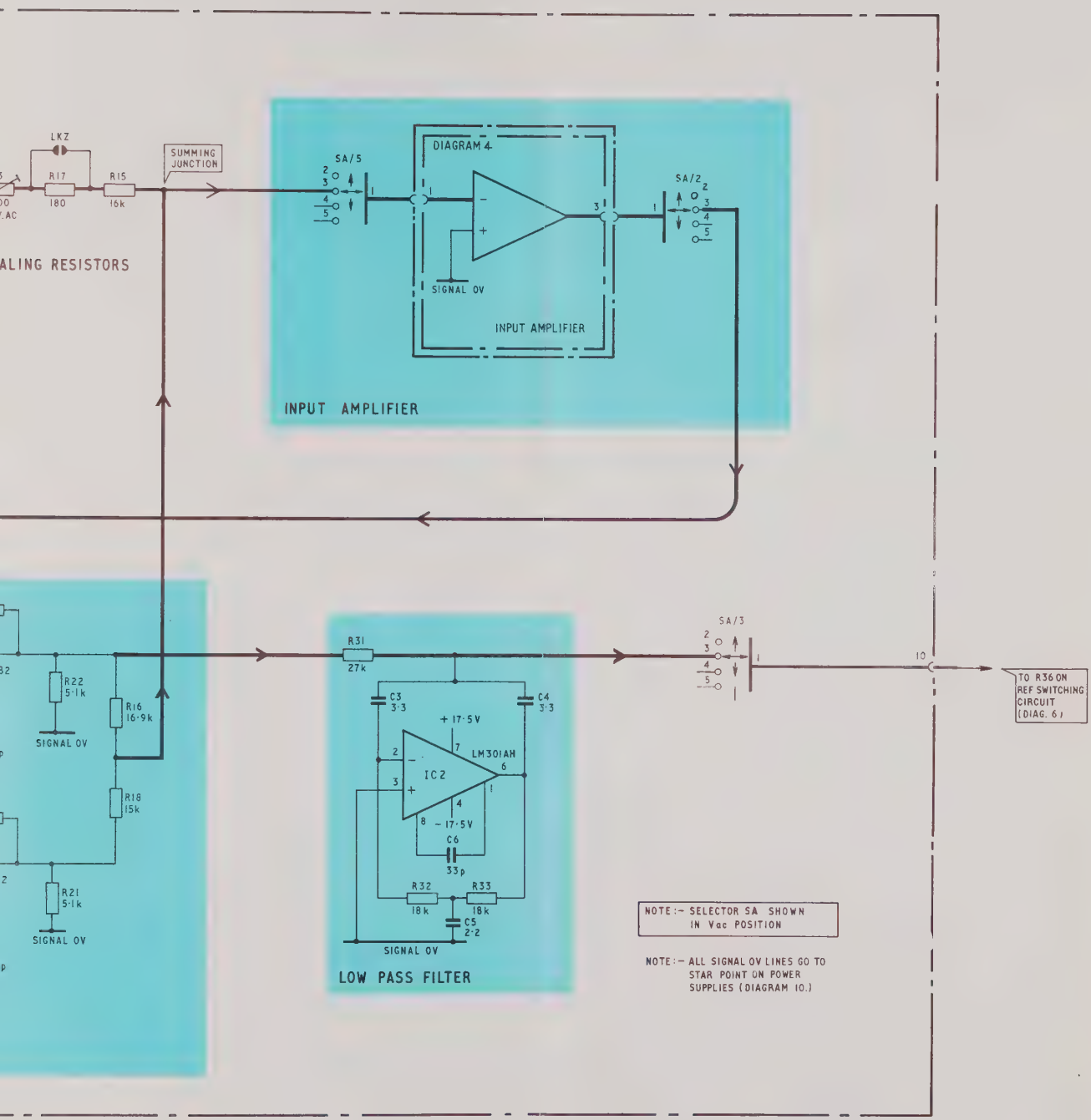
POS. COARSE REFERENCE SWITCH

If the COMPARATOR (DIAGRAM 7) detects a negative input signal during ramp-up, IC7-pin 16 goes low during the coarse ramp-down period. This turns on TR18 applying +10.000V as a positive reference input to discharge the level (proportional to the applied input signal) stored in the integrating capacitor C21 in the INTEGRATOR (DIAGRAM 7) during ramp-up.

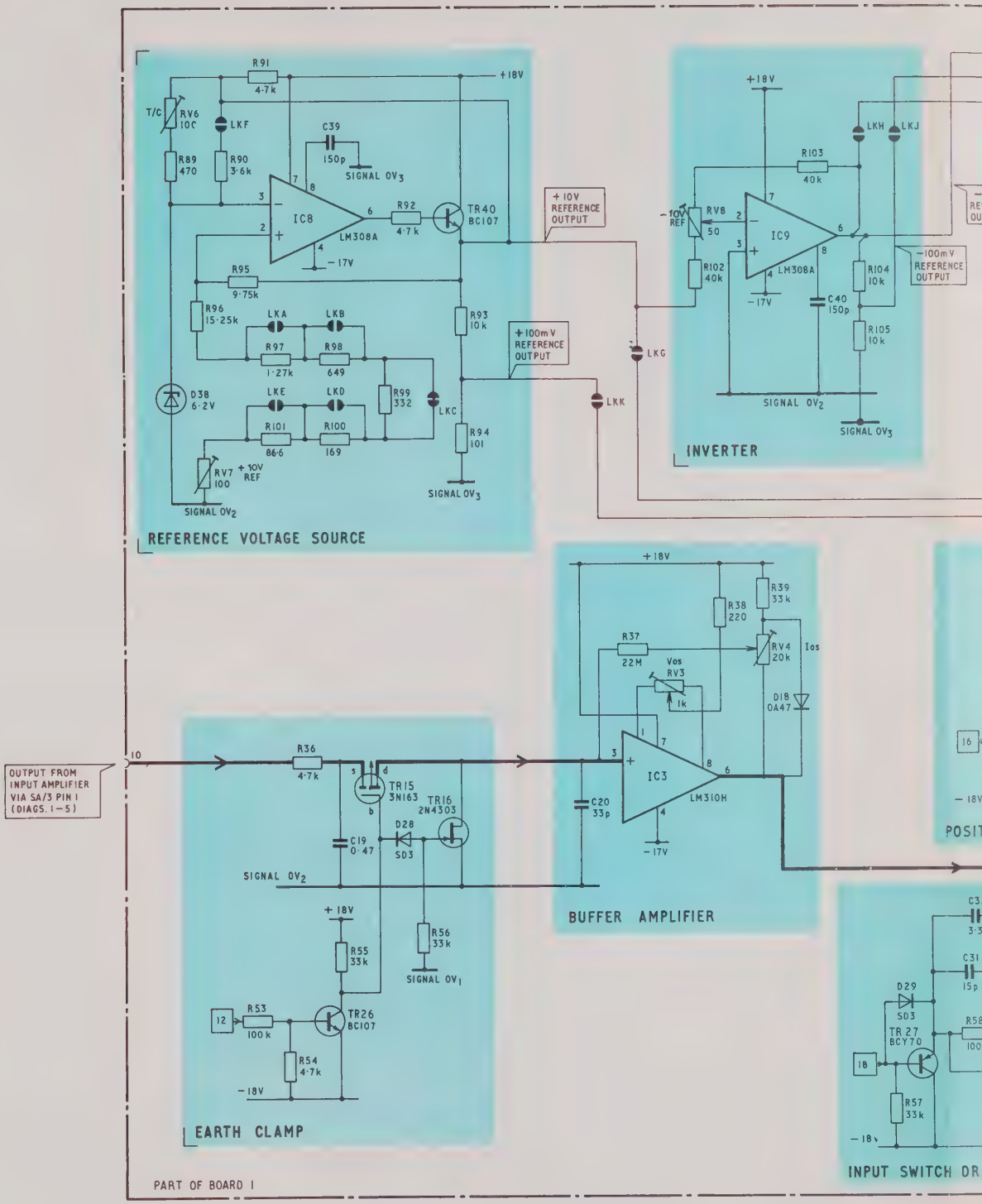
POS. FINE REFERENCE SWITCH

If the input signal was positive during ramp-up, IC7-pin 15 goes low, turning on TR22 during the fine ramp-down period to apply + 100mV as a fine reference signal to the INTEGRATOR (DIAGRAM 7).


PART OF FRONT PANEL
HI
Lo
GUARD
SA/1
SA/3
SA/4
C1
0·22
R12
990k
R13
2·2k
R11
10k
RLC/1
RLB/2
100V. AC
RV5
50
RV4
500
10V. AC
R10
100k
R9
1M
SIGNAL 0V
INPUT ATTENUATOR
+17·5V
C11
0·047
SIGNAL 0V
R14
100k
IC1
LM310H
C2
22
-17·5V
C12
0·047
SIGNAL 0V
A.C. AMPLIFIER
SIGNAL 0V
TO PIN 7 ON IC1 & IC2
TO T1 PIN 8 ON POWER SUPPLIES (DIAG. 10.) VIA GUARD PLATE
+17·5V FROM POWER SUPPLIES (DIAG. 10)
-17·5V FROM POWER SUPPLIES (DIAG. 10)
TO PIN 4 ON IC1 & IC2
TO SA/4 PIN 7 ON DIAG. 9
+17·5V
R27
470
D7
3·9V
TR1
BCY70
R29
27k
TR3
BC107
TR2
BC107
D9
9·1V
R30
1000
D8
3·9V
R28
220
D4
HP5082
R25
2·2k
R26
10k
D6
HP5082
R23
2·2k
R24
10k
RECTIFIER SYSTEM
PART OF BOARD 2



5 *AC MODE CIRCUIT DIAGRAM*


REFERENCE VOLTAGE SOURCE
INVERTER
BUFFER AMPLIFIER
EARTH CLAMP
INPUT SWITCH DR
PART OF BOARD 1
OUTPUT FROM INPUT AMPLIFIER VIA SA/3 PIN 1 (DIAGS. 1–5)
+18V
-17V
SIGNAL 0V2
SIGNAL 0V3
SIGNAL 0V1
+10V REFERENCE OUTPUT
+100mV REFERENCE OUTPUT
-100mV REFERENCE OUTPUT
IC8
LM308A
IC9
IC3
LM310H
TR40 BC107
TR15 3N163
TR16 2N4303
TR26 BC107
TR27 BCY70
D38 6·2V
D28 SD3
D29 SD3
D18 0A47
R91 4·7k
RV6 10C
R89 470
R90 3·6k
C39 150p
R92 4·7k
R95 9·75k
R96 15·25k
R97 1·27k
R98 649
R99 332
R100 169
R101 86·6
R93 10k
R94 101
RV7 100
R103 40k
R102 40k
RV8 50
R104 10k
R105 10k
C40 150p
R36 4·7k
C19 0·47
R55 33k
R56 33k
R53 100k
R54 4·7k
R37 22M
RV3 1k
RV4 20k
R38 220
R39 33k
C20 33p
LKA
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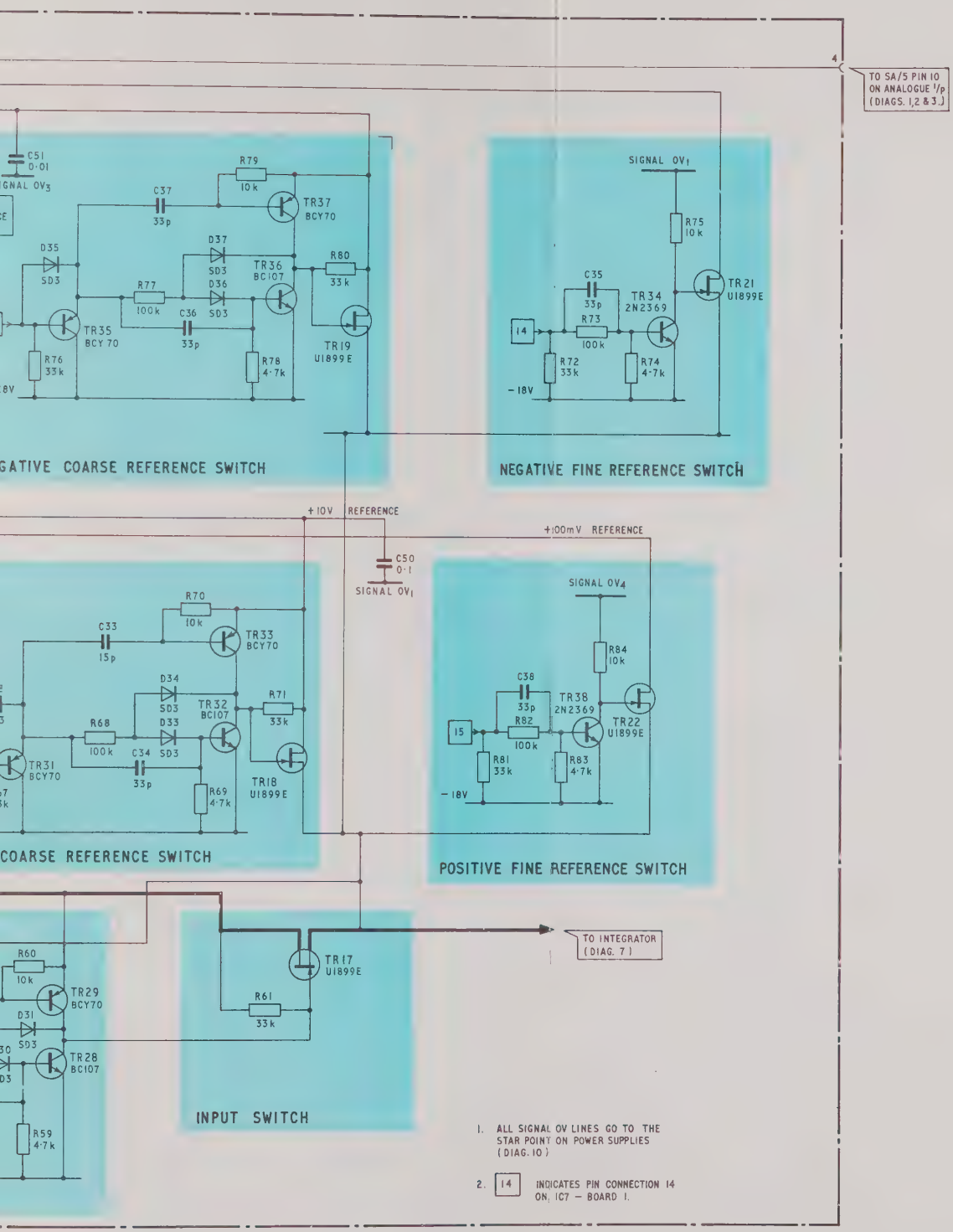
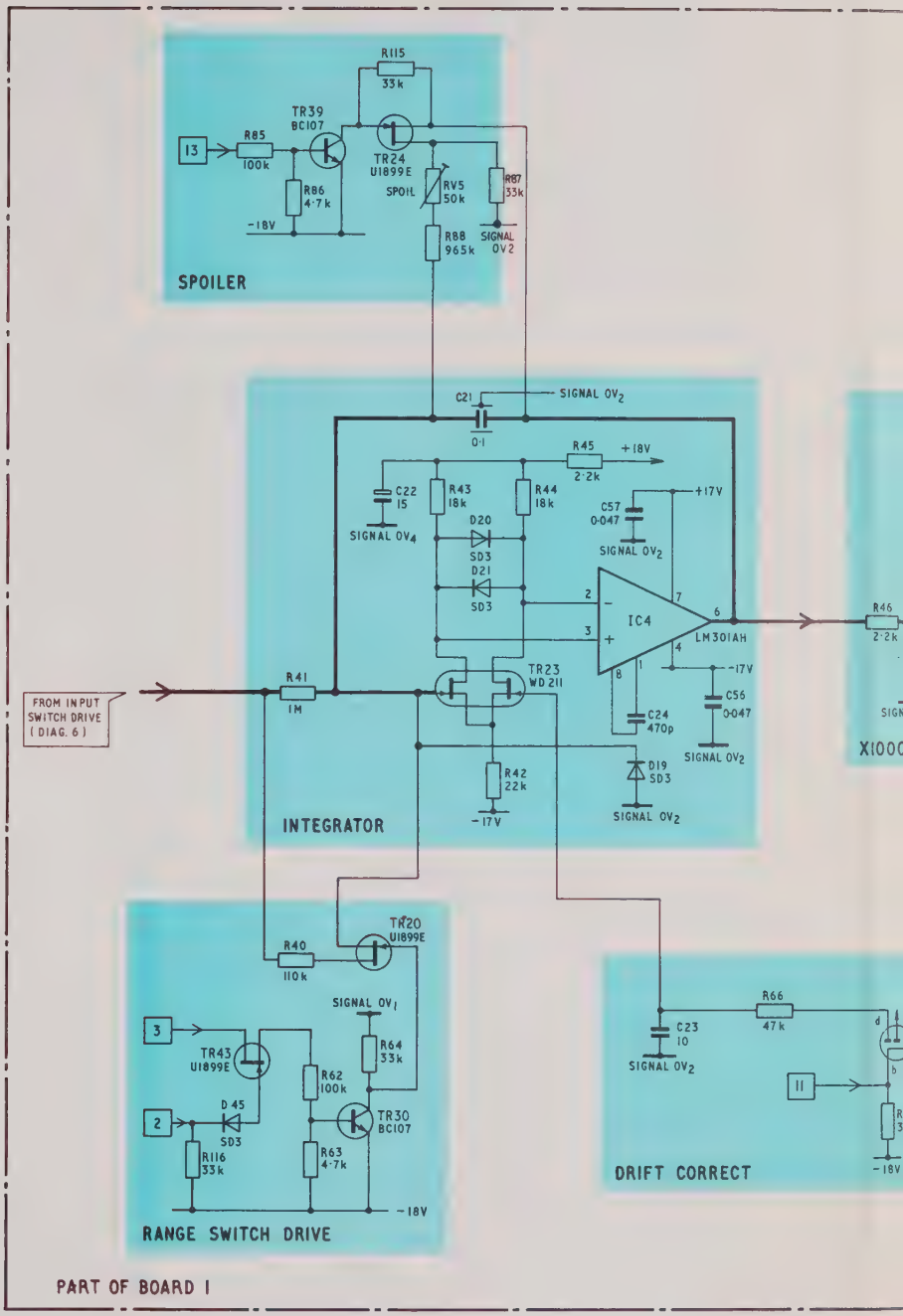
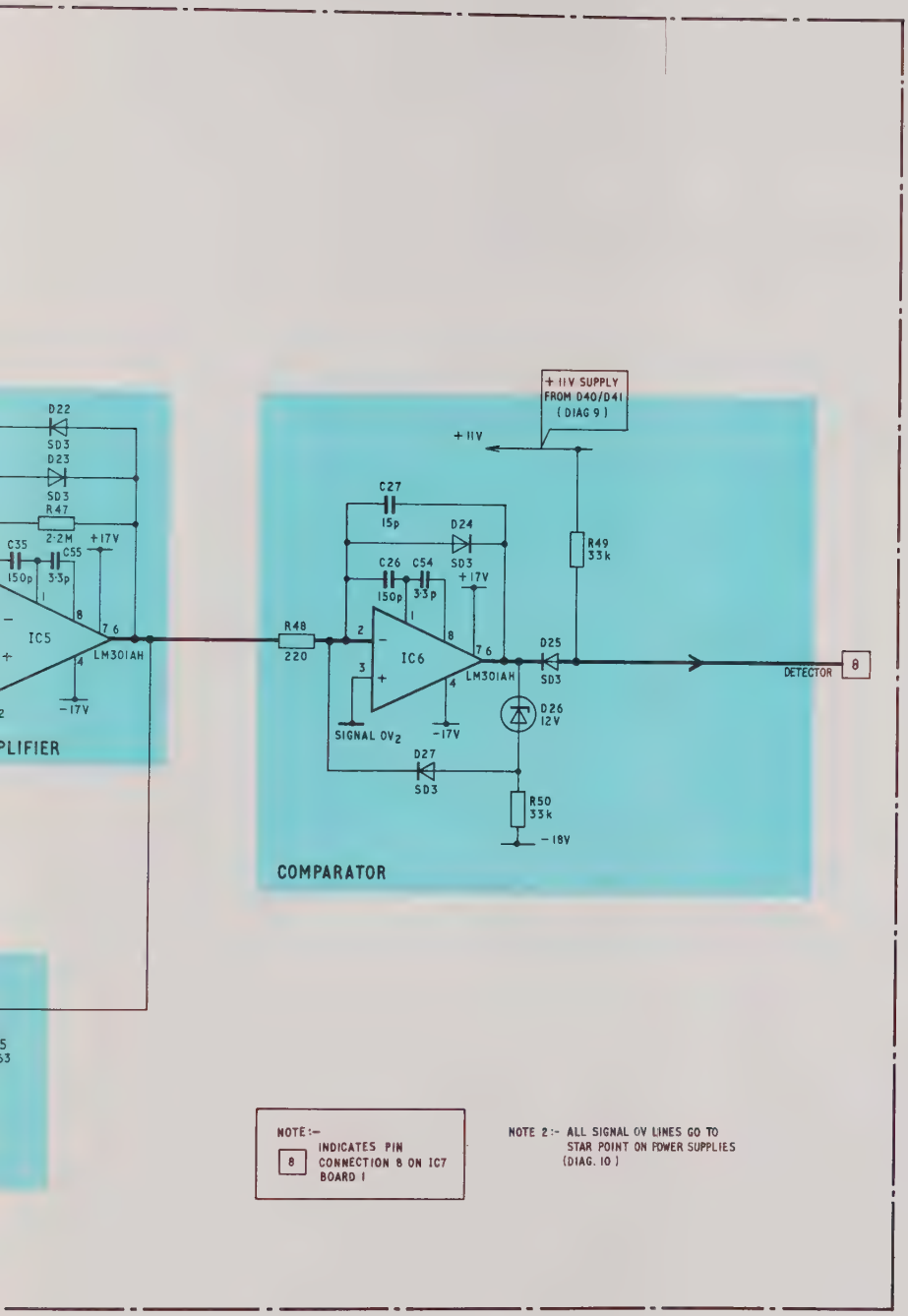
LKC
LKD
LKE
LKF
LKG
LKH
LKJ
LKK
T/C
Vos
Ios

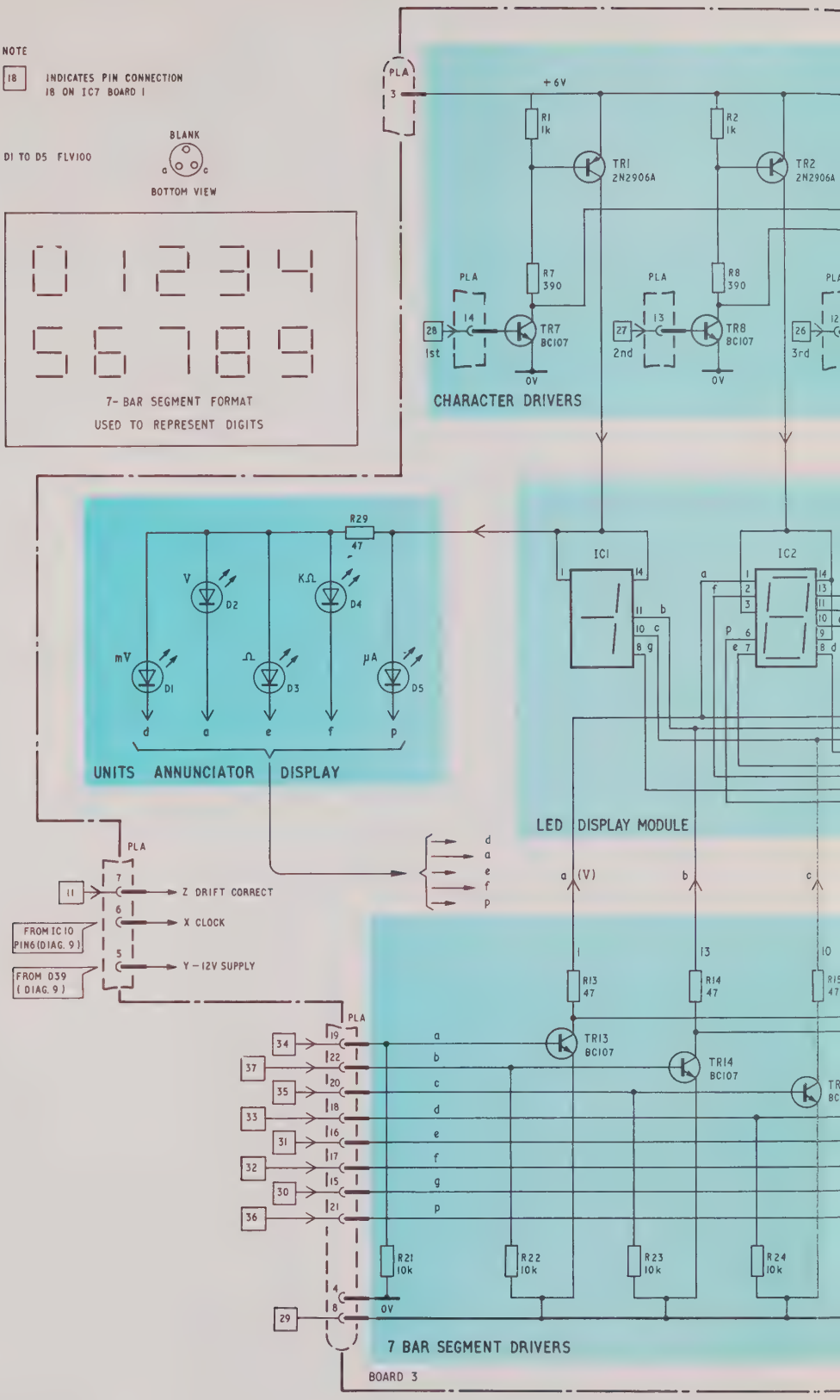


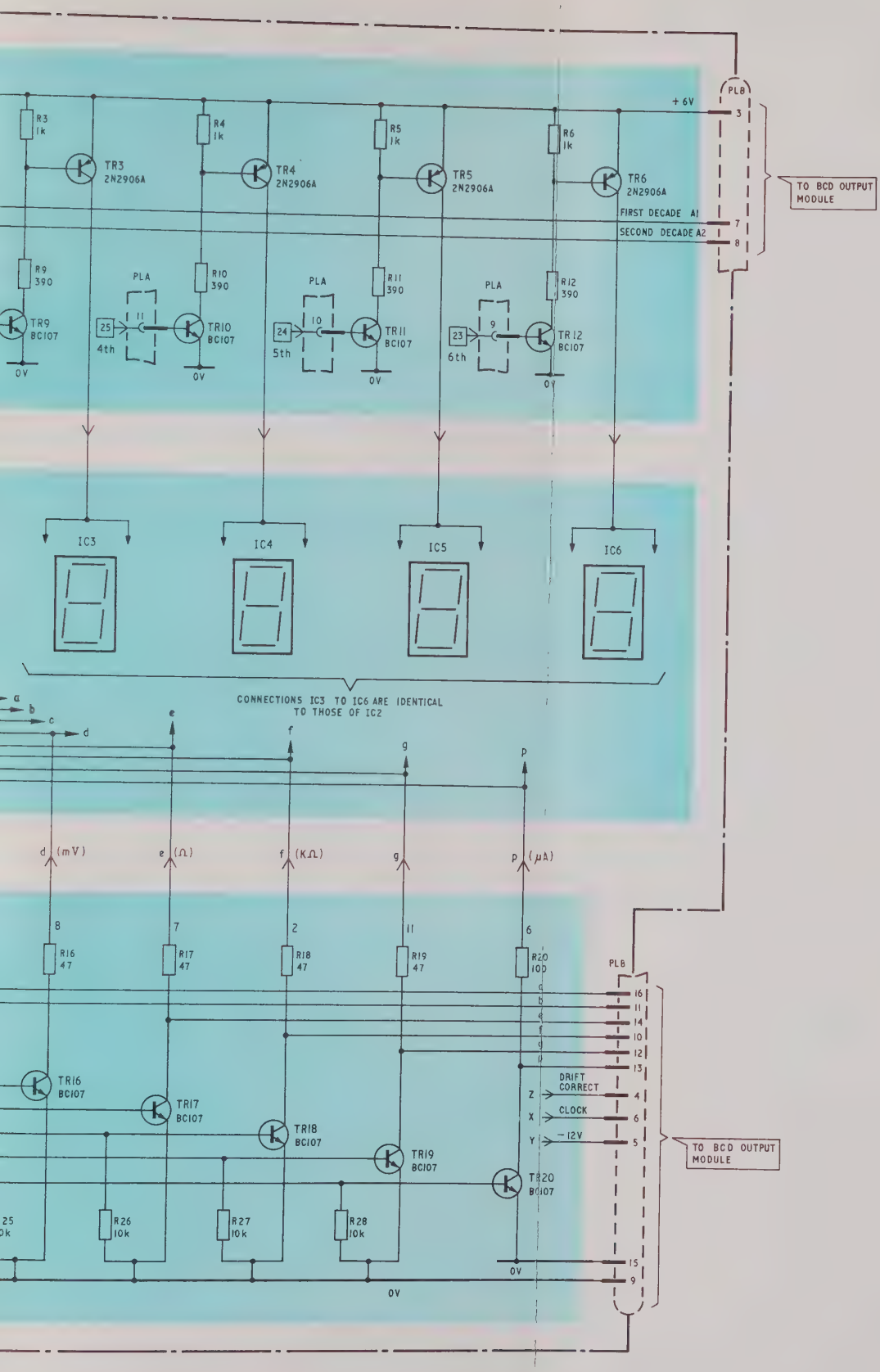
6 *REFERENCE SWITCHING CIRCUIT DIAGRAM*


SPOILER
R115
33k
TR39
BC107
R85
100k
13
TR24
U1899E
SPOIL
RV5
50k
R87
33k
R86
4·7k
-18V
R88
965k
SIGNAL
0V2
C21
0·1
SIGNAL 0V2
R45
2·2k
+18V
C22
15
SIGNAL 0V4
R43
18k
R44
18k
D20
SD3
D21
SD3
C57
0·047
SIGNAL 0V2
+17V
IC4
LM301AH
R46
2·2k
FROM INPUT
SWITCH DRIVE
(DIAG. 6)
R41
1M
TR23
WD211
-17V
C56
0·047
C24
470p
SIGNAL 0V2
R42
22k
-17V
D19
SD3
SIGNAL 0V2
INTEGRATOR
X1000
TR20
U1899E
R40
110k
SIGNAL 0V1
3
TR43
U1899E
R64
33k
R62
100k
D45
SD3
2
TR30
BC107
R116
33k
R63
4·7k
-18V
RANGE SWITCH DRIVE
R66
47k
C23
10
SIGNAL 0V2
11
-18V
DRIFT CORRECT
PART OF BOARD 1



7 INTEGRATOR CIRCUIT DIAGRAM


NOTE
18 INDICATES PIN CONNECTION 18 ON IC7 BOARD 1
D1 TO D5 FLV100
BLANK
BOTTOM VIEW
0 1 2 3 4
5 6 7 8 9
7- BAR SEGMENT FORMAT
USED TO REPRESENT DIGITS
PLA
+6V
R1 1k
R2 1k
TR1 2N2906A
TR2 2N2906A
R7 390
R8 390
TR7 BC107
TR8 BC107
1st
2nd
3rd
0V
CHARACTER DRIVERS
R29 47
V D2
KΩ D4
mV D1
Ω D3
μA D5
UNITS ANNUNCIATOR DISPLAY
IC1
IC2
LED DISPLAY MODULE
Z DRIFT CORRECT
X CLOCK
Y – 12V SUPPLY
FROM IC 10 PIN 6 (DIAG. 9)
FROM D39 (DIAG. 9)
R13 47
R14 47
TR13 BC107
TR14 BC107
R21 10k
R22 10k
R23 10k
R24 10k
7 BAR SEGMENT DRIVERS
BOARD 3



8 *DISPLAY CIRCUIT DIAGRAM*

CLOCK AND MODE SELECTION

CLOCK OSCILLATOR

A stable crystal controlled oscillator producing a source of timing pulses at 404kHz.

DIVIDE BY 4

A binary divider stage dividing the input signal by a factor of 4. The resultant output frequency of each output is 101kHz. Reference should be made to the text for details of the phase relationship between each output.

CLOCK DRIVERS

The input clock pulse train (101kHz) drives TR41 and TR42 on and off, forming output pulses between +11V and −17V (maximum amplitude = 28.5V) which are of sufficient amplitude to drive the clock inputs of IC7 (MOS - LSI circuit).

MODE SELECTION SWITCH

At each switch position, the appropriate input of IC7 will be held low thus selecting the appropriate mode. When VDC is selected, all the mode inputs go high and the DC mode is assumed.

RELAY DRIVE

Whenever IC7-pin 38 goes high, relay RLB is energised. Diode D10 (Bd. 2) provides a discharge path for the relay coil back emf when the relay is turned off. Whenever IC7 pin 2 is low TR13 is off and TR14 is on. Thus RLC is energised. Diode D11 (Bd. 2) provides a discharge path for the relay coil back emf when the relay is turned off.

AC Ranging Delay

When RLC is energised IC7 pin 6 drops to −17.5V on a time constant of C49, and 100k ohm (internal resistance in IC7), giving a delay of approximately two readings. D41 clamps C49 (+Ve) to Vss when RLC is de-energised.

IC7 (MOS - LSI) INTEGRATED CIRCUIT

IC7 is illustrated with its function identities and the diagram numbers on which these functions are effected.

The logic used by IC7 is as follows.

Positive Logic:-	Bar Drivers	Negative Logic:-	The remaining functions except the following:-
	IC Drivers (Characters)		Detector
	Top Range		Line Frequency
			Clock (ϕ_1 and ϕ_2)
			Supply Rails

Supply Rail voltages are:-

Vss = 11V Nominal

Vdd = −18V Nominal

Vee = 0V

NOTES:-

1. Terminals marked N/A are not used and must not be connected to any other part of the circuitry.
2. Before attempting to remove this MOS Integrated Circuit ensure that all power supplies are switched off and that the necessary anti-static charge measures are taken. See warning on page 3b-5.

SUB SECTION 3c Power Supplies

This sub-section deals with the POWER SUPPLIES section of the instrument whose primary function is to provide all the internal dc levels required to operate the instrument.

POWER SUPPLIES

GENERAL ARRANGEMENT

This section of circuitry provides all the dc voltage levels required to operate the instrument.

0V Rails.

Within the instrument, the common return paths (0V rails) are carefully separated to reduce interference. Care should be taken not to short these rails together other than where shown.

Split Pads LKL and LKM (pcb No. 1)

These pads enable the user to isolate the stabilised supplies from the associated section of circuitry. Since these pads are continuations of the printed circuit copper work, care should be taken not to overheat these connections causing the track to lift away from the board.

50/60Hz SHAPER

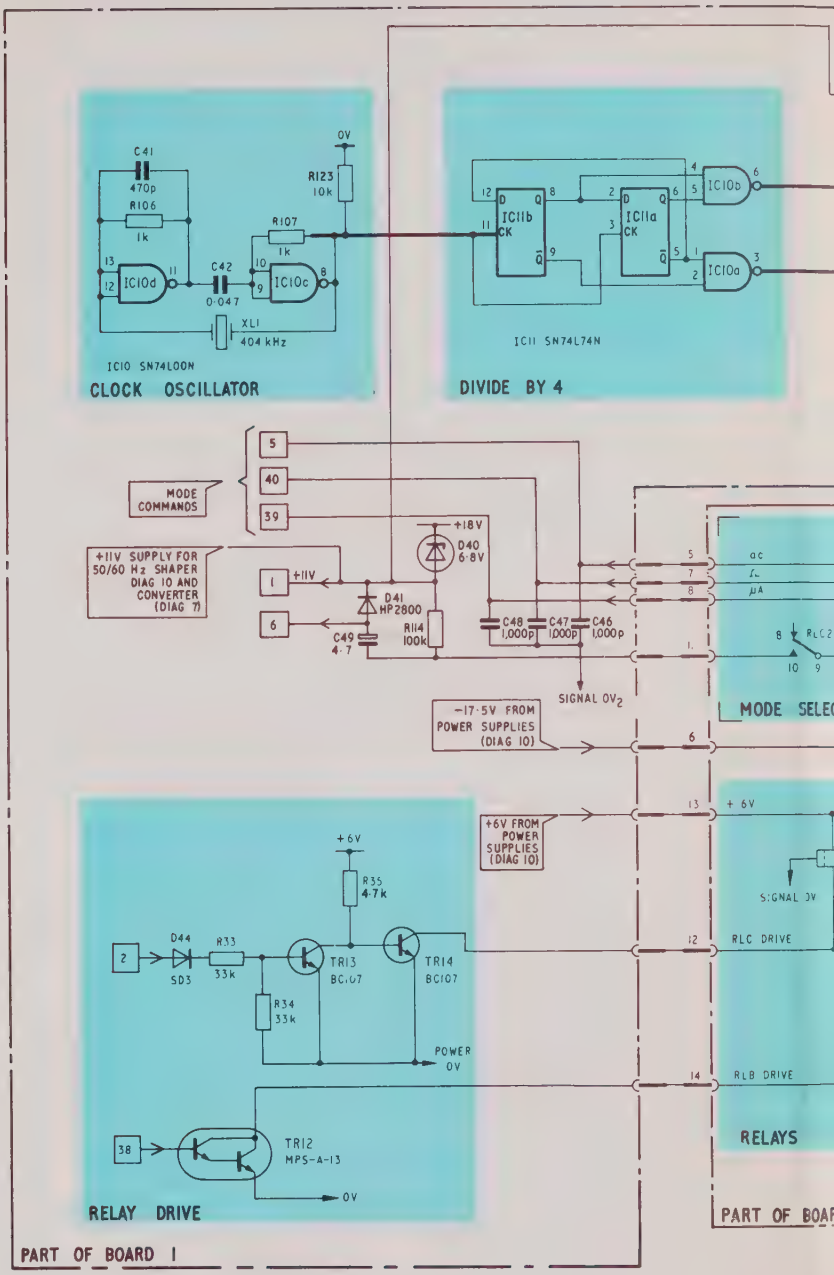
A small proportion of the incoming mains frequency is sampled; the signal is clipped and is used by IC7 (MOS-LS1 circuit) to provide mains zero timing reference points.

VOLTAGE RAIL USAGE

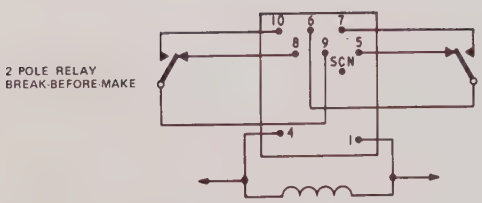
The following table gives the nominal rail voltages provided and the circuit diagrams on which they appear.

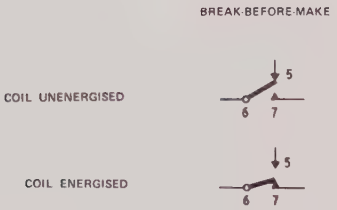
+18V	4, 6, 7, 9
−18V	4, 6, 7, 9, 10
+17.5V	4, 5
−17.5V	4, 5, 9
+17V	7,
−17V	6, 7
+6V	8, 9

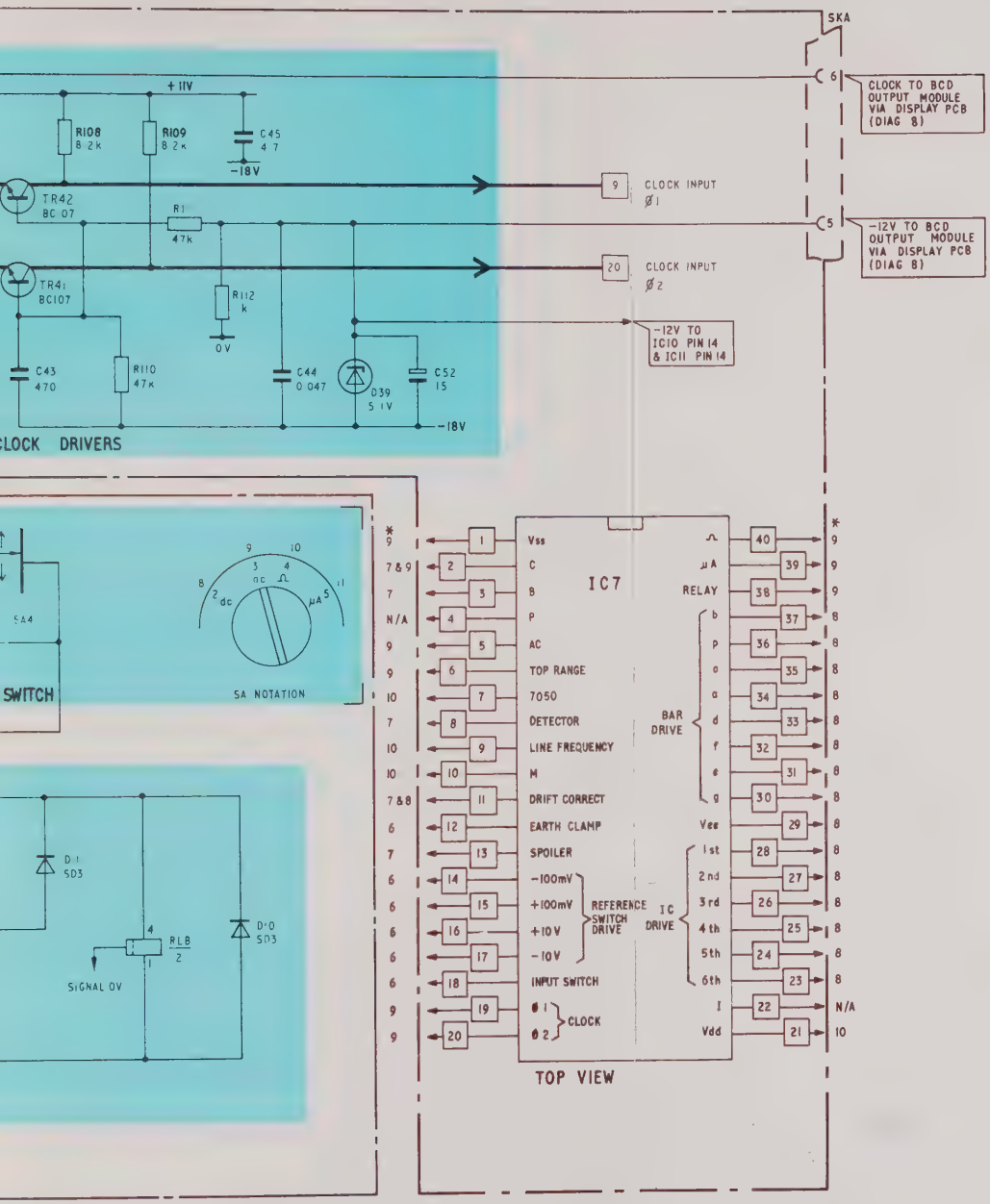
A nominal 10V rms output is available from transformer T1, terminals 5 and 6 for use on the BCD Output Module.



NOTES:—
1. RELAY CONTA
5 AC MODE
1-3 ANALOG
9 MODE SE
2. [2] INDICA
2 ON
3. ALL 0V AN
GO TO STAR
SUPPLIES (D
4. NUMBERS U
DIAGRAMS W

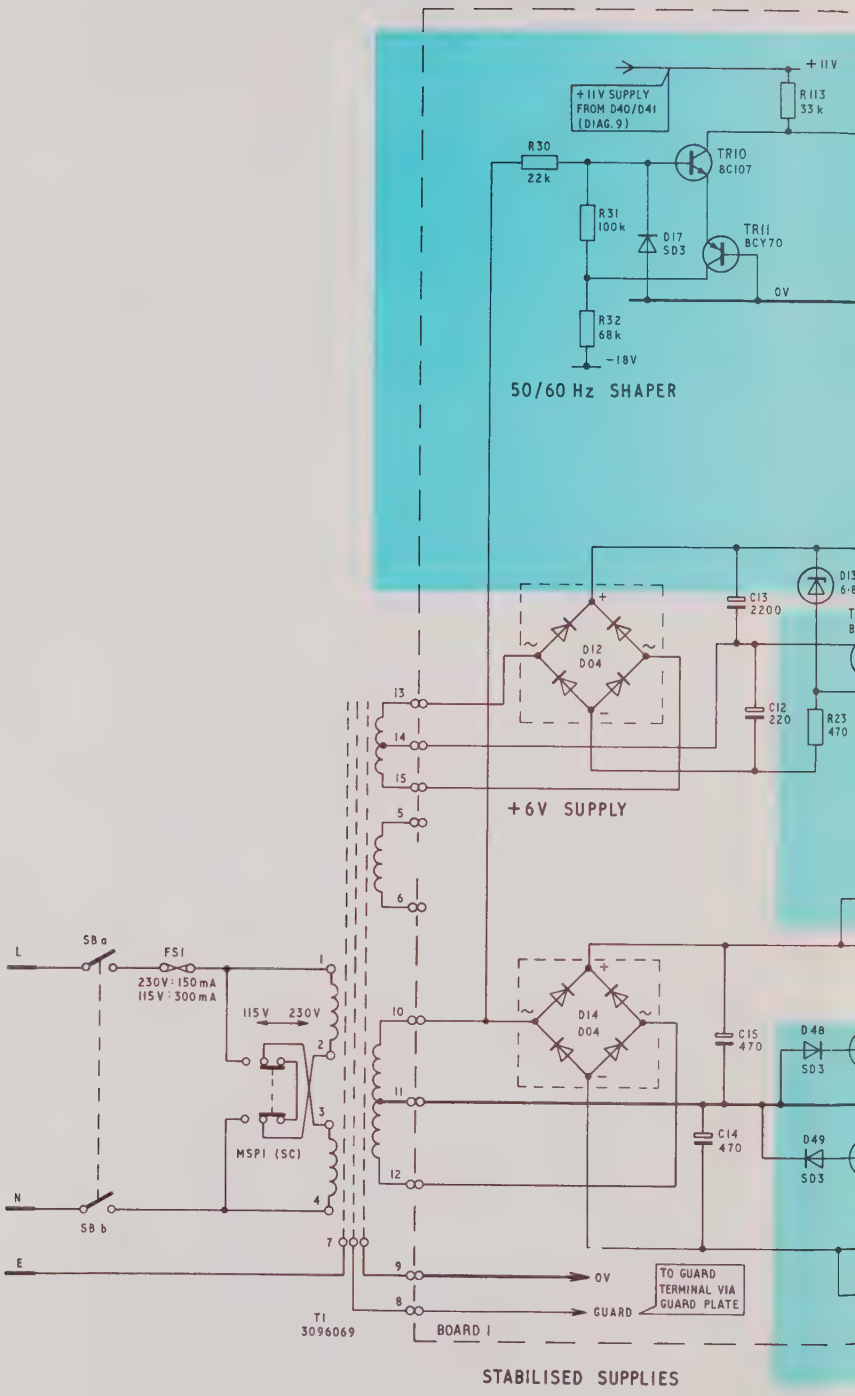


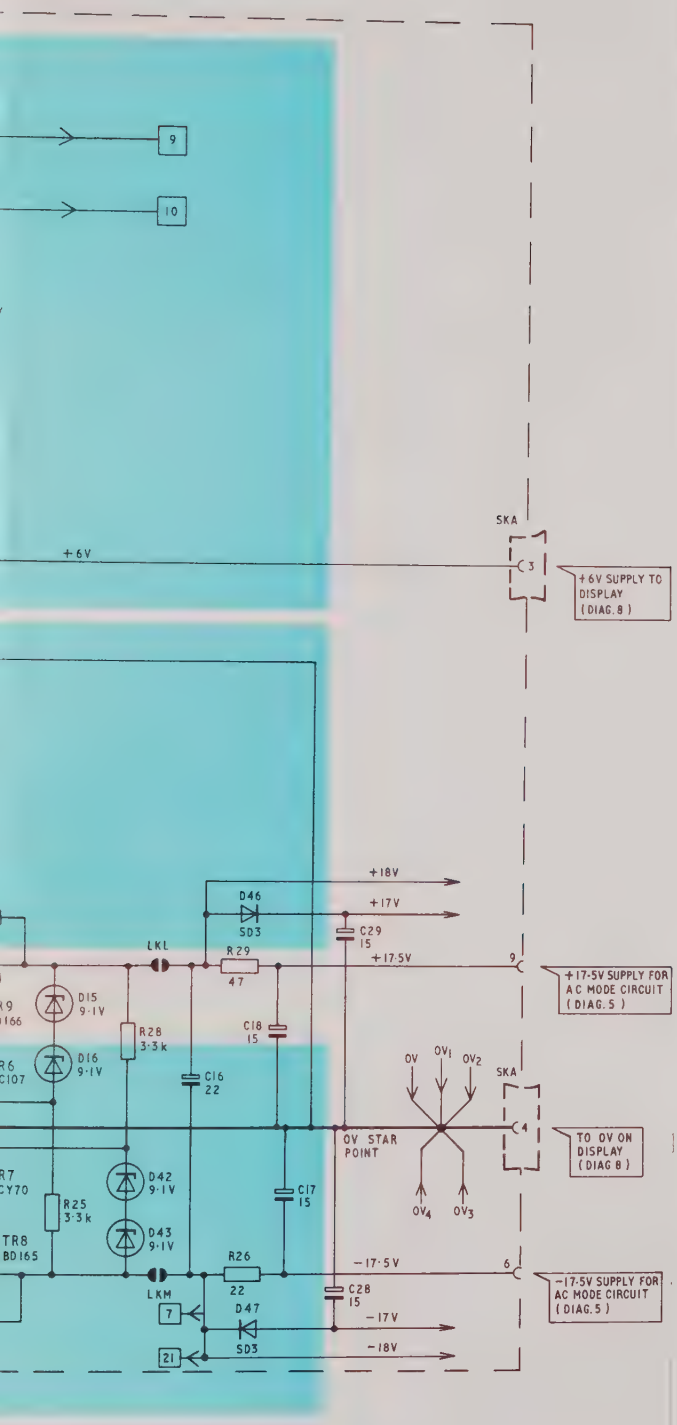




SHOWN ON DIAGRAMS
_C1
T RLB 1
_C2
CONNECTION
RD 1
0V LINES
ON POWER
DENOTE
E AFFECTED

9 CLOCK AND MODE SELECTION CIRCUIT DIAGRAM


+11V
+11V SUPPLY FROM D40/D41 (DIAG. 9)
R113 33k
R30 22k
TR10 BC107
R31 100k
D17 SD3
TR11 BCY70
0V
R32 68k
-18V
50/60 Hz SHAPER
D12 D04
C13 2200
C12 220
R23 470
+6V SUPPLY
L
SB a
FS1
230V: 150mA
115V: 300mA
115V 230V
MSP1 (SC)
N
SB b
E
D14 D04
C15 470
C14 470
D48 SD3
D49 SD3
0V
GUARD
TO GUARD TERMINAL VIA GUARD PLATE
T1 3096069
BOARD 1
STABILISED SUPPLIES



10 *POWER SUPPLIES CIRCUIT DIAGRAM*

SECTION 4 Setting Up & Calibration

INTRODUCTION

This section provides a comprehensive setting-up and calibration procedure which may be necessary after a rectification and/or component replacement on the Digital Multimeter.

It is divided into two parts as follows.

1. Setting-Up Procedures

   These involve partial strip down of the instrument in order to effect initial adjustments of the circuit parameters.

2. Calibration Procedures

   The final adjustments to provide an instrument performance which is compatible with the specification published in Section 6 of this manual.

   For a normal calibration only Part 2 of this section needs to be carried out. Where an instrument fails a calibration, or has had a rectification and/or component replacement, it is advisable to carry out the full procedure detailed in this section.

NOTE:- It is essential when carrying out Part 1 or 2, that the procedure be completed, and carried out in the order given.

TEST EQUIPMENT

The test equipment used must have an accuracy uncertainty equal to or better than that shown in the calibration test tables.

The following test equipment should be available to perform the following procedures correctly.

(a) Variac.

(b) Digital Voltmeter (e.g. Type 7040).

(c) Oscilloscope Type 1740 or A100.

(d) Decade Resistance Standard (e.g. ESI Model RS624).

(e) AC Voltage Standard (e.g. Hewlett Packard Models 745A and 746A).

(f) Decade Voltage Divider (e.g. ESI Model RV622A).

(g) AC Source (e.g. Bradley 232).

(h) DC Source (e.g. Time Model 2003, ± 0.02%).

(j) DC Voltage Standard (e.g. Kintel 351).

(k) Thermal Probe (ambient + 20^{o}C).

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(g) AC Source (e.g. Bradley 232).

(h) DC Source (e.g. Time Model 2003, ± 0.02%).

(j) DC Voltage Standard (e.g. Kintel 351).

(k) Thermal Probe (ambient + 20°C).

(l) Additional items:- Resistor, 1k ohm ± 10% (0.125W).

Resistor, 27k ohm ± 10% (0.125W).

Resistor, 1M ohm ± 10% (0.125W).

Capacitor 1μF (non-polarised).

PART 1. SETTING UP PROCEDURES

PRELIMINARY

1. Prepare the instrument as follows:-

CAUTION:- IT IS ESSENTIAL THAT THE INSTRUMENT BE ISOLATED FROM THE MAINS SUPPLY BEFORE OUTER CASE REMOVAL, DUE TO THE UNCOVERED TERMINALS ON THE ON/OFF SWITCH.

CAUTION:- BEWARE OF GUARD POTENTIAL ON GUARD PLATE WITH INSTRUMENT CASE REMOVED.

a. Remove the 4, 2.5mm screws holding the outer case to the rear panel assembly, Fig. 4.1.

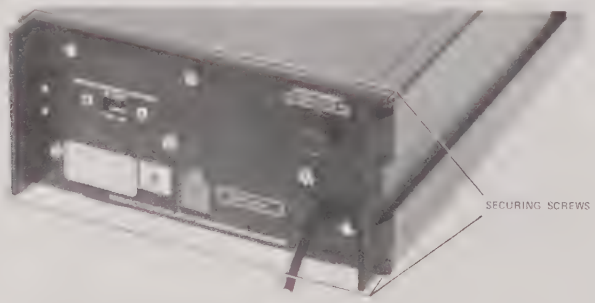


Fig. 4.1. View of Rear Panel, showing location of the 4 securing screws.

b. Select the 'V.DC' mode (This orientates the selector switch shaft with it's key flat facing upwards).

c. Remove the GUARD - Lo link (if fitted).

d. Gently ease out the pcb and rear panel assembly away from the front panel. Fig. 4.5, at rear of section, shows the location and function of each potentiometer.

e. Remove the 2 sets of Berg pins and the 4 screws attaching pcb 2 to pcb 1. Remove pcb 2.

2. Link Berg socket 2 to Berg socket 10.

3. Check that the Mains Selector in the rear panel is set to the appropriate voltage, and that the correct rated fuse is fitted.

For	230V:-	150mA	SLO BLO FUSE
	115V:-	300mA	SLO BLO FUSE

4. Apply power to the instrument and allow a sufficient warm up period.

5. Check that the rail voltages are within the limits specified over the input voltage range as follows.

For	230V:-	195.5 to 253 Volts.
	115V:-	97.75 to 126.5 Volts.

TEST BETWEEN	LIMITS OVER MAINS VARIATION	
	MINIMUM	MAXIMUM
C16 (+ve) to C18 (–ve)	+16.5V	+18V
C16 (–ve) to C18 (–ve)	–16.5V	–18V
C13 (+ve) to C18 (–ve)	+6.0V	+7.0V
C45 (+ve) to C45 (–ve)	+25V	+30V
C52 (+ve) to C52 (–ve)	+4.75V	+5.25V

REFERENCE TEMPERATURE COEFFICIENT

NOTE:- The potentiometer involved is RV6. Once set, great care must be exercised during the remainder of the procedure to prevent inadvertant adjustment of this potentiometer.

1. Select 'V.DC' mode. Remove link from Berg sockets 2 and 10 and apply –10V ± 0.1% absolute between them (negative to 10), using a DC Standard having a ½ hour stability of less than 5ppm.

2. Attach a variable resistance box (100k ohms to 1 ohm) between R96/R97 and C22 (–ve) of pcb 1. Adjust resistance box for a reading of 100.000 ± 10 bits.

3. Increase ambient temperature at D38 by 20°C (application of a Thermal Probe to D38 or by other means). Adjust RV6 and/or link LKF for 100.000 reading.

4. Allow D38 temperature to return to ambient and re-adjust resistance box for a reading of 100,000 ± 10 bits.

5. Re-apply heat of ambient + 20°C ± 4°C. Reading should change by less than ± 5 bits. Repeat adjustments until change is less than ± 5 bits. Remove the –10V supply and resistance box.

BUFFER Vos Ios

1. Select 'V.DC' mode. Short circuit Berg sockets 2 and 10. Connect voltmeter between Berg socket 2 and D18 cathode, via a 1k ohm resistor.

2. Adjust RV3 for 0 ± 20μV on voltmeter. Replace the link between Berg sockets 2 and 10 by a 27k ohm resistor.

3. Adjust RV4 for 0 ± 10μV on the voltmeter. Remove voltmeter and two resistors (27k ohm and 1k ohm).

SPOILER

1. Select 'V.DC' mode. Link Berg sockets 4 and 10.

2. Connect TR26 collector (case) via a 33k ohm resistor to TR10 collector (case) and note instrument reading.

3. Remove the resistor connection and adjust RV5 to obtain the reading noted in (2) above.

4. Remove the 33k ohm resistor and the link between Berg sockets 4 and 10.

POSITIVE REFERENCE

Select 'V.DC' mode. Apply −10V and −1V, using the DC Standard and the Decavider, to Berg sockets 2 and 10 (−ve to 10) and adjust RV7 to share the error between −10,0000V (± 2 bits) and −1.00000 (± 2 bits) readings evenly.

NOTE:- If RV7 does not have enough adjustment the links will require re-adjustment as follows:-

a. Connect −10V (± 0.02% absolute) from DC Standard to Berg sockets 2 and 10 (Common to socket 2).

b. Ensure that links LKA to LKE inclusive are open circuit and that RV7 is at maximum resistance (fully clockwise).

c. Apply −10V standard and note the reading. Look up the range which includes this reading in Table 4.1 and set links LKA to LKE accordingly.

READING RANGES		LINKS				
		A	B	C	D	E
100000	100199	1	1	1	1	1
100172	100373	1	1	1	1	0
100337	100540	1	1	1	0	1
100513	100718	1	1	1	0	0
100669	100876	1	1	0	1	1
100848	101056	1	1	0	1	0
101020	101230	1	1	0	0	1
101202	101414	1	1	0	0	0
101332	101546	1	0	1	1	1
101517	101734	1	0	1	1	0
101696	101914	1	0	1	0	1
101885	102105	1	0	1	0	0
102053	102276	1	0	0	1	1
102246	102471	1	0	0	1	0
102431	102658	1	0	0	0	1
102628	102858	1	0	0	0	0
102704	102935	0	1	1	1	1
102904	103137	0	1	1	1	0
103096	103331	0	1	1	0	1
103299	103537	0	1	1	0	0
103481	103721	0	1	0	1	1
103689	103931	0	1	0	1	0
103888	104134	0	1	0	0	1
104101	104349	0	1	0	0	0
104252	104502	0	0	1	1	1
104469	104721	0	0	1	1	0
104677	104932	0	0	1	0	1
104897	105156	0	0	1	0	0
105094	105355	0	0	0	1	1
105320	105583	0	0	0	1	0
105537	105803	0	0	0	0	1
105767	106037	0	0	0	0	0

Legend

0 = Short Circuit

Table 4.1.

d. Repeat the −10V and −1V test as detailed previously.

RE-ASSEMBLY

1. Fit pcb 2 to pcb 1, securing it by the 4 screws.

2. Fit the link between GUARD and LO terminals and insert the 2 sets of Berg pins into their sockets, ensuring they are fully engaged.

INPUT AMPLIFIER

NOTE:- The waveform at TR3 collector, using a dc coupled oscilloscope set to 1V/cm and 1ms/cm, should be a square wave; amplitude 4V ± 0.4Vpp, period 4ms ± 1ms, mark/space ratio 1 : 1 ± 10%.

1. Select 'V.DC' mode and short circuit the input terminals. Ensure that RV1 range of adjustment is greater than ± 80μV.

2. Remove the short circuit from the input terminals. Apply +100μV and −100μV alternately to the input terminals, using a dc source having an output resistance of 10k ohms.

3. Adjust RV1 for equal positive and negative readings.

4. Remove dc source and connect a 1M ohm resistor and 1μF non-polarised capacitor in parallel between the Hi and Lo terminals.

5. Adjust RV2 for a zero reading, ± 10μV. Remove resistor and capacitor.

6. Recheck the Input Amplifier zero, (short circuiting the input terminals as in operation 1 above) and the ± 10V, (using the DC Standard across the input terminals) readings limits.

   These are:- ± 10μV ± 1 bit for zero input.

   ± 10V ± 2 bits for the 10V input.

   NOTE:- If adjustment is necessary repeat operations 2 to 5 inclusive.

7. Remove the dc source.

NEGATIVE REFERENCE

1. Select 'V.DC' mode.

2. Connect 10V ± 0.02% absolute across the 6 decade Decavider, using the DC Standard.

3. Apply +10V, −10V, +1V and −1V dc in turn to the input terminals.

4. Adjust on RV8 to make the negative reading equal to the positive reading at each voltage level.

5. Share errors between RV7 and RV8 such that the:-

   ± 10V readings are ± 10.0000V ± 2 bits

   ± 1V readings are ± 1.00000V ± 2 bits

   NOTE:- Problems in meeting these limits will result if the 'ON' resistance of TR's 17, 18, 19 and 20 are not matched. See Appendix.

LINEARITY

1. Select 'V.DC' mode. With the 10V DC Standard and Decavider connected to the input terminals as in previous test, check the linearity in accordance with Table 4.2.

INPUT	READING	TOLERANCE
10V	10.0000V	± 3 bits
5V	5.0000V	± 2 bits
1.05V	1.0500V	± 2 bits
0.95V	*950.00mV	± 2 bits
1.05V	1.05000V	± 2 bits
1.15V	*1.1500V	± 2 bits
0.5	*500.00mV	± 2 bits
0.1	100.00mV	± 2 bits
0.01	10.00mV	± 2 bits
0.001	1.00mV	± 2 bits
0.0001	0.10mV	± 2 bits
0.00005	0.05mV	± 2 bits
0.00003	0.03	± 2 bits
0.00002	0.02mV	± 2 bits
0.00001	0.01mV	± 2 bits

* = Range Change

Table 4.2

2. Repeat for negative values using the same voltage source.

3. If the DMM falls outside the linearity tolerances, it is recommended that the Setting Up Procedure should be repeated.

OHMS MODE

1. Set to 'Ω' mode and short circuit the input terminals. The reading should be less than 3 bits.

2. Connect 100k ohms ± 0.01% absolute across the input terminals. Adjust RV2 (pcb 2) and/or link LKY to obtain 100.000kΩ reading.

DC ATTENUATOR

Select 'V.DC' mode and connect input terminals to 100V ± 0.01% absolute. Adjust RV1 (pcb 2) and/or link LKX to give 100.000V reading.

DC μA

Select 'μA.DC' mode and connect input to 1000μA ± 0.01% absolute current source (100k ohms from 100V is convenient). Adjust RV6 (pcb 2) to give 1000.00μA ± 10 bits reading.

AC ZERO

Switch to 'V.AC' mode. Short circuit TR1 (pcb 2) collector (case) to 0V. Adjust RV4 until the readings stop reducing. Reading must be less than 5 bits. Remove the short circuit.

AC SCALE

1. Select 'V.AC' mode. Connect the input to 1V ± 0.1% absolute 1kHz sinewave. On pcb 2, adjust RV3 and link LKZ to give 1.00000V, with at least ± 50 bit adjustment on RV3.

AC ATTENUATOR

1. Select 'V.AC' mode. Connect the input to 10V ± 0.2% absolute 1kHz sinewave. Adjust RV4 (pcb 2) to obtain 10.0000V ± 50 bits.

2. Increase the input to 100V ± 0.2 absolute 1kHz sinewave. Adjust RV5 (pcb 2) to obtain 100.000V ± 50 bits.

INTERFERENCE REJECTION

SERIES MODE

1. Connect instrument as shown in Fig. 4.2.

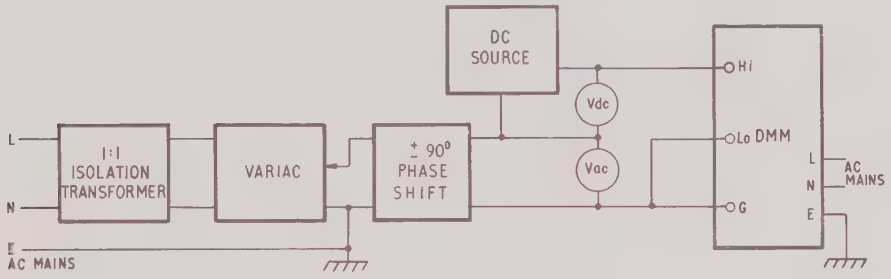


Fig. 4.2. Interference Rejection:- Series Mode Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to approximately 500mV and (V.ac) to zero. Note the instrument reading.

3. Increase (V.ac) to 1 Volt. Reading must not change by more than 1mV.

COMMON MODE

AC Rejection

1. Connect instrument as shown in Fig. 4.3.

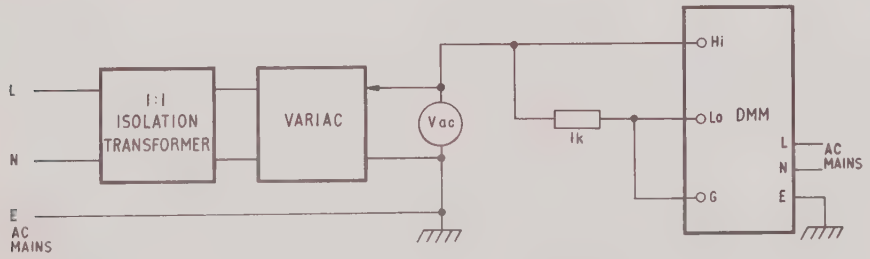


Fig. 4.3. Interference Rejection:- Common Mode (ac) Test Circuit.

2. Switch to 'V.AC' mode and set (V.ac) to 100V. Reading shall be less than 100mV.

DC Rejection

1. Connect instrument as shown in Fig. 4.4.

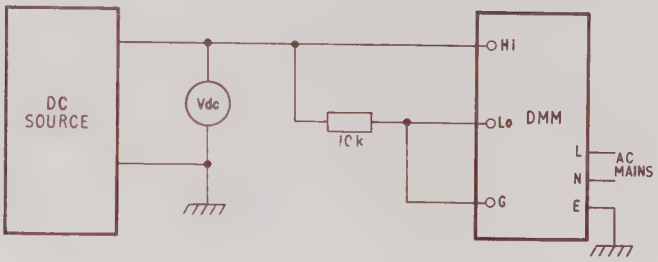


Fig. 4.4. Interference Rejection:- Common Mode (dc) Test Circuit.

2. Switch to 'V.DC' mode and set (V.dc) to 500V. Reading shall be less than 5mV.

This concludes the setting up of the DMM and it should now be followed by a full calibration.

PART 2. CALIBRATION PROCEDURES

INTRODUCTION

The following calibration is basically the final calibration to which all instruments are subjected, prior to despatch from the factory.

For the greatest accuracy the DMM should be removed from its case and fitted into a Setting Up Case, Part No. 70502 before a calibration is attempted. Failing this, allowances must be made for variations in the working temperatures.

See Appendix for details of Setting Up Case.

PRELIMINARY PROCEDURE

The DMM will have to be removed from its case and fitted into the Setting Up Case (if available).

CAUTIONARY NOTES

1. IT IS ESSENTIAL THAT THE INSTRUMENT BE COMPLETELY ISOLATED FROM THE MAINS SUPPLY BEFORE REMOVING THE CASE, DUE TO THE POSITION AND UNPROTECTED NATURE OF THE ON/OFF SWITCH TERMINALS.

2. BEWARE OF THE GUARD PLATE POTENTIAL WITH INSTRUMENT CASE REMOVED.

1. Remove the 4, 2.5mm screws which secure the DMM case to the rear panel. See Fig. 4.1.

2. Remove the GUARD - Lo link (if fitted).

3. Gently ease out the rear panel and pcb assembly, away from the front panel.

4. Fit assembly into the Setting Up Case (if available), or position assembly in convenient position with the guard plate insulated if required and with easy access to the potentiometers.

5. Ensure that the correct mains selection has been made and that the correct rated fuse is fitted.

   For 230V:- 150mA SLO BLO

   115V:- 300mA SLO BLO

CALIBRATION

The calibration sequence must be carried out in the order given. Calibration should be carried out at an ambient temperature $23^{\circ}C \pm 1^{\circ}C$ after a warm-up period of approximately half an hour in the Setting-Up Case.

STANDARD SETTINGS

During the warm up period the DMM should be set to the following standard conditions.

1. Mode set to 'V.DC'.

2. Input terminals short circuited.

3. Apply power to the DMM and switch instrument ON.

CALIBRATION PROCEDURE 1

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	1MΩ//1μF	10	Adj. Bd.1/RV2.	± 0.00mV	2	
2	S/C	–	Adj. Bd.1/RV1.	± 0.00mV	0	
3	1MΩ//1μF	10	Adj. Bd.1/RV2.	± 0.00mV	10	
4	+0.10mV	2	Adj. Bd.1/RV1 and repeat for equal +ve and –ve readings.	0.10mV	2	
5	–0.10mV	2		–0.10mV	2	
6	S/C	–	Check.	± 0.00mV	2	
7	+10.0000V	0.001	Adj. Bd.1/RV7. (1)	10.0000V	-2	
8	+10.0000V	0.001	Check, with 1MΩ in series.	10.0000V	50	
9	–10.0000V	0.001	Adj. Bd.1/RV8. (1)	–10.0000V	3	

NOTES:-

(1) Adjust for equal reading, split any deviations equally between readings.

CALIBRATION PROCEDURE 2

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	105.000kΩ	0.001	Adj. Bd.2/RV2.	105.000kΩ	5	
2	50.000kΩ	0.002	Check.	50.000kΩ	9	
3	5kΩ	50	Range change.	5.0000kΩ		
4	10.5000kΩ	0.002	Check.	10.5000kΩ	10	
5	5.0000kΩ	0.005	Check.	5.0000kΩ	15	
6	1.0500kΩ	0.005	Check.	1.0500kΩ	7	
7	500.0Ω	0.01	Check.	500.0Ω	6	
8	O/C	–	Overload Check. (1)	1–––––kΩ	–	
9	S/C	–	Check.	0.0Ω	5	

NOTES:-

(1) Ensure that overload condition is indicated by a steady '1' being displayed and that the remaining 5 characters are blanked out.

CALIBRATION PROCEDURE 3

Select 'V.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	+10.0000V	0.001	Check.	10.0000V	3	
2	+1.0500V	0.002	Check.	1.0500V	2	
3	+0.5V	50	Range change.	500.00mV		
4	+1.05000V	0.001	Check.	1.05000V	5	
5	+105.00mV	0.002	Check.	105.00mV	2	
6	+10.00mV	0.02	Check.	10.00mV	2	
7	−10.0000V	0.001	Check.	−10.0000V	4	
8	−1.0500V	0.002	Check.	−1.0500V	2	
9	−0.5V	50	Range change.	−500.00mV		
10	−1.05000V	0.001	Check.	−1.05000V	5	
11	−105.00mV	0.002	Check.	−105.00mV	2	
12	−10.00mV	0.02	Check.	−10.00mV	2	
13	+105.000V	0.001	Adj. Bd.2/RV1.	105.000V	2	
14	+1000.00V	0.005	Check.	1000.00V	10	
15	−105.00V	0.002	Check.	−105.00V	3	

CALIBRATION PROCEDURE 4

Select 'Ω' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	1.05000MΩ	0.005	Check.	1050.00kΩ	20	
2	500.00kΩ	0.005	Check.	500.00kΩ	15	
3	10.0000MΩ	0.01	Check.	10000.0kΩ	150	
4	5.0000MΩ	0.01	Check.	5000.0kΩ	100	

CALIBRATION PROCEDURE 5

Select 'μA.DC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	O/C	–	Check.	0.000μA	4	
2	+1.00000mA (1)	0.005	Adj.Bd.2/RV6. (6)	1000.00μA	30	
3	+9μA (2)	10	Range change.	9.000	900	
4	+10.000μA (3)	0.005	Check.	10.000μA	6	
5	+1.000μA (4)	0.05	Check.	1.000μA	4	
6	–20V	10	Overload check. (5)	–1————μA	–	
7	–1.00000mA (1)	0.005	Check.	–1000.00μA	35	
8	–9μA	10	Range change.	–9.000	900	
9	–10.000μA (3)	0.005	Check.	–10.000μA	8	
10	–1.000μA (4)	0.05	Check.	–1.000μA	4	

NOTES:-

(1) Recommend 100V source via a 100k ohm resistor.

(2) Recommend 9V source via a 1M ohm resistor.

(3) Recommend 10V source via a 1M ohm resistor.

(4) Recommend 1V source via a 1M ohm resistor.

(5) Ensure that overload is indicated by flashing '1' with the remaining 5 characters blanked out.

(6) For adjustment of this potentiometer the case must be removed.

CALIBRATION PROCEDURE 6

Select 'V.AC' on Mode Selector

TEST	INPUT		OPERATION	READING		RESULT
	VALUE	±%		VALUE	± bits	
1	1.00000V	0.02	At 1kHz. Adjust Bd.2/RV3.	1.00000V	20	
2	1.00mV	1	At 1kHz. Check.	1.00mV	9	
3	S/C	–	Check.	0.00	9	
4	500.00mV	0.02	At 1kHz. Check.	500.00mV	20	
5	100.00mV	0.02	At 1kHz. Check.	100.00mV	15	
6	1.00000V	0.05	At 40Hz. Check.	1.00000V	100	
7	1.00000V	0.05	At 20kHz. Check.	1.00000V	200	
8	1.00000V	0.02	At 10kHz. Check.	1.00000V	100	
9	100.00mV	0.02	At 20kHz. Check.	100.00mV	18	
10	10.0000V	0.02	At 1kHz. Adjust Bd.2/RV4. (1)	10.0000V	20	
11	100.000V	0.02	At 1kHz. Adjust Bd.2/RV5. (1)	100.000V	20	
12	1.2000V	0.02	At 1kHz. Check.	1.2000V	20	
13	10.0000V	0.02	At 10kHz. Check.	10.0000V	150	
14	100.000V	0.02	At 10kHz. Check.	100.000V	150	
15	750.00V	0.05	At 1kHz. Check.	750.00V	50	
16	500.00V	0.05	At 10kHz. Check.	500.00V	100	
17	10.0000V	0.02	At 10kHz. Check.	10.0000V	150	

NOTES:-

(1) For adjustment of this potentiometer the case must be removed.

This concludes the calibration of the DMM. If the instrument fails any of the prescribed tests it is suggested that the Setting Up Procedures in Section 4 be carried out, followed by a further calibration before any fault diagnosis is attempted.

The serviceable DMM should now be isolated from the supplies and refitted into its case.

NOTE:- Ensure that 'V.DC' is selected on both the switch and the front panel knob to ensure correct mating of the key flat.

Potentiometer RV5 (SPOIL)

Sets the Spoiler (DIAG. 7) time constant.

Potentiometer RV2 (Lo. Ω)

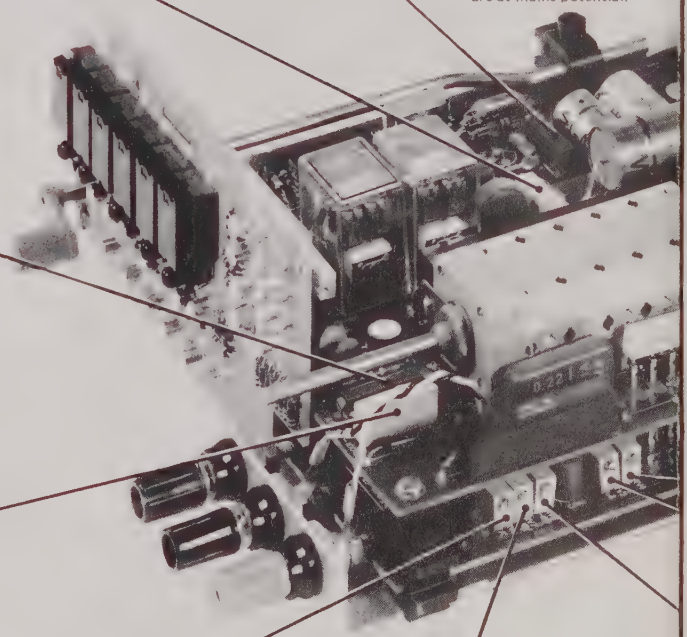
Defines the 100μA reference current from 10V reference in 'Ω' mode (DIAG. 2).

Potentiometer RV6 (μA)

Sets the 1000μA scaling (DIAG. 3).

HIGH VOLTAGE WARNIN

Bare terminals on this switch are at mains potential.



Potentiometer RV4 (10V.AC)

Sets the 10V ac scaling (DIAG. 6).

Potentiometer RV5 (100V.AC)

Sets the 100V ac scaling (DIAG. 6).

Potentiometer RV6 (T/C)

Adjusts the temperature coefficient of the positive reference voltage by controlling the current through D38 (DIAG. 7).

Potentiometer RV7 (+10V)

Sets the +10V reference voltage output for coarse ramp down (DIAG. 7).

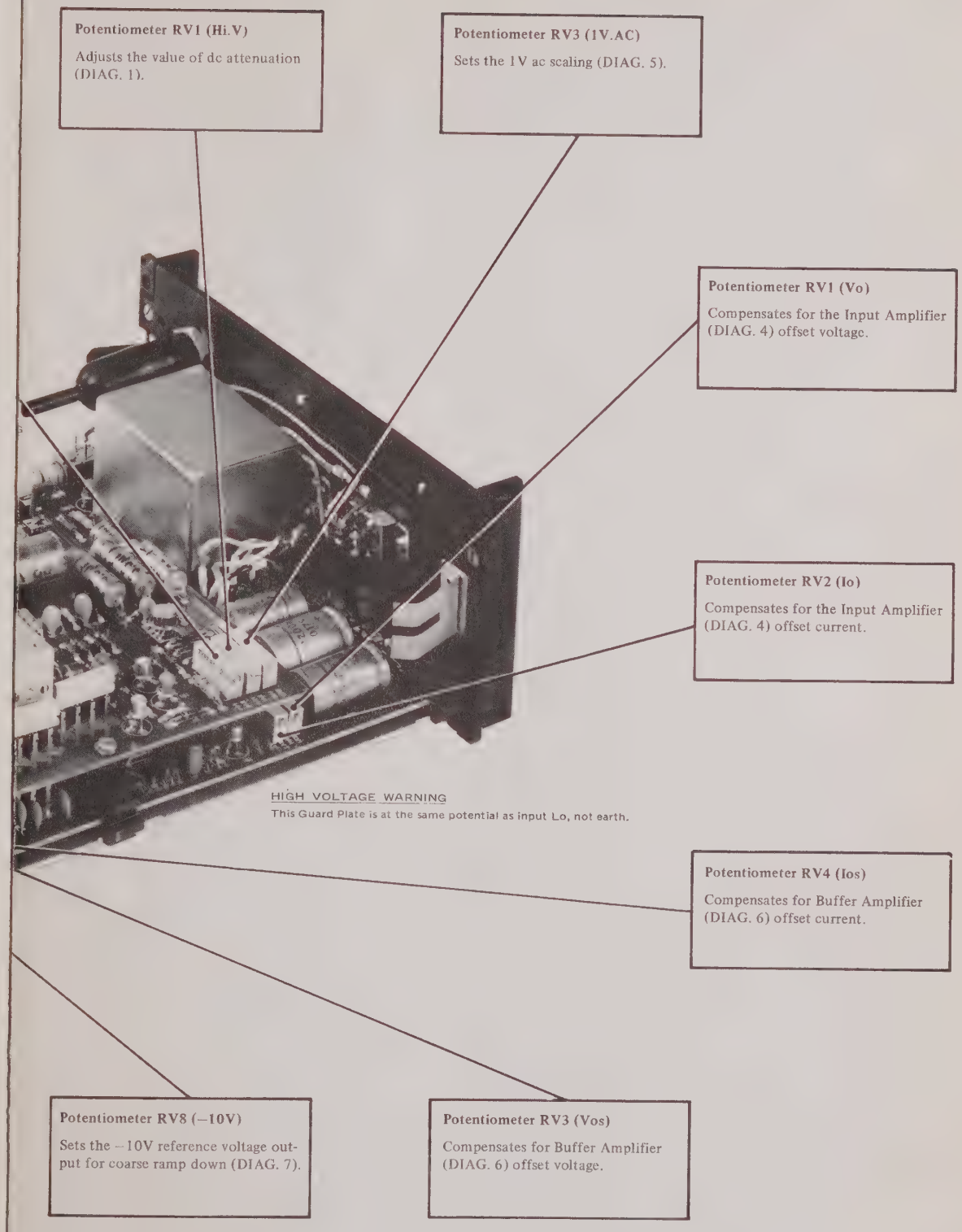

Potentiometer RV1 (Hi.V)
Adjusts the value of dc attenuation (DIAG. 1).
Potentiometer RV3 (1V.AC)
Sets the 1V ac scaling (DIAG. 5).
Potentiometer RV1 (Vo)
Compensates for the Input Amplifier (DIAG. 4) offset voltage.
Potentiometer RV2 (Io)
Compensates for the Input Amplifier (DIAG. 4) offset current.
HIGH VOLTAGE WARNING
This Guard Plate is at the same potential as input Lo, not earth.
Potentiometer RV4 (Ios)
Compensates for Buffer Amplifier (DIAG. 6) offset current.
Potentiometer RV8 (−10V)
Sets the −10V reference voltage output for coarse ramp down (DIAG. 7).
Potentiometer RV3 (Vos)
Compensates for Buffer Amplifier (DIAG. 6) offset voltage.

Fig. 4.5. View of PCB Assembly, identifying the Potentiometers and their Functions.

SECTION 5 Parts Lists

This section contains detailed parts lists for each of the printed circuit boards fitted in the instrument. When ordering spare parts, it is essential to quote the instrument serial number, located on the rear panel, as well as the full description shown in the appropriate parts list.

COMPONENT PARTS LIST

ABBREVIATIONS

Circuit References

B	Battery
C	Capacitor (μF)
CSR	Thyristor
D	Diode
FS	Fuse
IC	Integrated Circuit
L	Inductor
LP	Lamp (including Neon)
LK	Link
M	Meter
MSP	Mains Selector Panel
PL	Plug
R	Resistor (Ω)
RL	Relay
S	Switch
SK	Socket
T	Transformer
TP	Terminal Post (or Test Point)
TR	Transistor
V	Valve
X	Other Components

Also Used:-

RNL	Non Linear Resistor (Ω)
RV	Variable Resistor (Ω)

Component Composition

FIXED RESISTORS

Carbon Composition	CACP
Carbon Film	CAFM
Cracked Carbon	CKCA
Metal Film	MEFM
Metal Oxide	MEOX
Power Wirewound	POWW
Precision Wirewound	PRWW
Temperature Sensitive	TEMP
Thick Film	TKFM
Thin Film	TNFM
Voltage Sensitive	VOLT

Component Composition (Cont'd)

VARIABLE RESISTORS

Wirewound Preset Single Turn	WWPS
Wirewound Preset Multiturn	WWPM
Wirewound Front Panel Single Turn	WWFS
Wirewound Front Panel Multiturn	WWFM
Carbon Preset Single Turn	CAPS
Carbon Preset Multiturn	CAPM
Carbon Front Panel Single Turn	CAFS
Carbon Front Panel Multiturn	CAFM
Cermet Preset Single Turn	CMPS
Cermet Preset Multiturn	CMPM
Cermet Front Panel Single Turn	CMFS
Cermet Front Panel Multiturn	CMFM

CAPACITORS

Air	AIR
Aluminium Electrolytic	ALME
Aluminium Solid	ALMS
Polycarbonate	CARB
Ceramic	CERM
Polyester Foil	ESTF
Polyester Metallised	ESTM
Glass	GLAS
Mica	MICA
Metallised Lacquer	MLAC
Paper Foil	PAPF
Paper Metallised	PAPM
PTFE	PTFE
Polypropylene Film	PYLN
Polystyrene	STYR
Tantalum Dry	TAND
Tantalum Foil	TANF
Tantalum Wet	TANW

PCB No. 1

Cct Ref	General Description				Solartron Part No.
R1	CACP	1000	1/8W	10%	172031000
R2	CACP	470	1/8W	10%	172024700
R3	CACP	47k	1/8W	10%	172044700
R4	CACP	47k	1/8W	10%	172044700
R5	CACP	10	1/8W	10%	172011000
R6	CACP	1.5M	1/8W	10%	172061500
R7	CACP	220k	1/8W	10%	172052200
R8	CACP	22	1/8W	10%	172012200
R9	CACP	220k	1/8W	10%	172052200
R10	CACP	10k	1/8W	10%	172041000
R11	CACP	220k	1/8W	10%	172052200
R12	CACP	220k	1/8W	10%	172052200
R13	CACP	100	1/8W	10%	172021000
R14 to R19	MEOX	22k	1/4W	5%	195642200
R20	MEOX	9.1k	1/4W	5%	195639100
R21	MEOX	9.1k	1/4W	5%	195639100
R22	MEOX	100k	1/4W	5%	195651000
R23	MEOX	470	1/2W	5%	193524700
R24	CACP	3.3k	1/4W	10%	172333300
R25	CACP	3.3k	1/4W	10%	172333300
R26	CACP	22	1/8W	10%	172012200
R27	CACP	3.3k	1/4W	10%	172333300
R28	CACP	3.3k	1/4W	10%	172333300
R29	CACP	47	1/8W	10%	172014700
R30	CACP	22k	1/8W	10%	172042200
R31	CACP	100k	1/8W	10%	172051000
R32	CACP	68k	1/8W	10%	172046800
R33	CACP	33k	1/8W	10%	172043300
R34	CACP	33k	1/8W	10%	172043300
R35	CACP	4.7k	1/8W	10%	172034700
R36	CACP	4.7k	1/8W	10%	172034700
R37	CACP	22M	1/4W	10%	172372200
R38	CACP	220	1/8W	10%	172022200
R39	CACP	33k	1/8W	10%	172043300
R40	MEFM	110k	1/4W	0.5%	198251101
R41	MEFM	1M	1/4W	1%	198361002
R42	MEOX	22k	1/4W	5%	195642200
R43	MEFM	18k	1/8W	0.5%	192741802
R44	MEFM	18k	1/8W	0.5%	192741802
R45	CACP	2.2k	1/8W	10%	172032200
R46	CACP	2.2k	1/8W	10%	172032200
R47	CACP	2.2M	1/8W	10%	172062200
R48	CACP	220	1/8W	10%	172022200
R49	CACP	33k	1/8W	10%	172043300
R50	CACP	33k	1/8W	10%	172043300
R53	CACP	100k	1/8W	10%	172051000
R54	CACP	4.7k	1/8W	10%	172034700
R55	CACP	33k	1/8W	10%	172043300
R56	CACP	33k	1/8W	10%	172043300
R57	CACP	33k	1/8W	10%	172043300
R58	CACP	100k	1/8W	10%	172051000
R59	CACP	4.7k	1/8W	10%	172034700
R60	CACP	10k	1/8W	10%	172041000
R61	CACP	33k	1/8W	10%	172043300
R62	CACP	100k	1/8W	10%	172051000
R63	CACP	4.7k	1/8W	10%	172034700
R64	CACP	33k	1/8W	10%	172043300
R65	CACP	33k	1/8W	10%	172043300
R66	CACP	47k	1/8W	10%	172044700
R67	CACP	33k	1/8W	10%	172043300
R68	CACP	100k	1/8W	10%	172051000
R69	CACP	4.7k	1/8W	10%	172034700
R70	CACP	10k	1/8W	10%	172041000
R71	CACP	33k	1/8W	10%	172043300
R72	CACP	33k	1/8W	10%	172043300
R73	CACP	100k	1/8W	10%	172051000
R74	CACP	4.7k	1/8W	10%	172034700
R75	CACP	10k	1/8W	10%	172041000
R76	CACP	33k	1/8W	10%	172043300
R77	CACP	100k	1/8W	10%	172051000
R78	CACP	4.7k	1/8W	10%	172034700

Cct Ref.	General Description				Solartron Part No.
R79	CACP	10k	1/8W	10%	172041000
R80	CACP	33k	1/8W	10%	172043300
R81	CACP	33k	1/8W	10%	172043300
R82	CACP	100k	1/8W	10%	172051000
R83	CACP	4.7k	1/8W	10%	172034700
R84	CACP	10k	1/8W	10%	172041000
R85	CACP	100k	1/8W	10%	172051000
R86	CACP	4.7k	1/8W	10%	172034700
R87	MEFM	33k	1/8W	0.5%	192743302
R88	MEFM	965k	1/4W	0.5%	160400530
R89	MEFM	470	1/4W	0.5%	198224701
R90	MEFM	3.6k	1/8W	0.5%	192733602
R91	CACP	4.7k	1/8W	10%	172034700
R92	CACP	4.7k	1/8W	10%	172034700
R93	MEFM	10k	1/8W	.25%	192841002
R94	MEFM	101	1/8W	.25%	192821012
R95	PRWW	9.75k	1/4W	0.1%	169606901
R96		15.25k	1/4W	0.1%	
R97	MEFM	1.27k	1/8W	1%	160400430
R98	MEFM	649	1/8W	1%	160400420
R99	MEFM	332	1/8W	1%	160400419
R100	MEFM	169	1/8W	1%	160400418
R101	MEFM	86.6	1/8W	1%	160400417
R102 & R103	PRWW	40k	1/4W	0.05%	169607001
R104	MEFM	10k	1/8W	.25%	192841002
R105	MEFM	101	1/8W	.25%	192821012
R106	CACP	1000	1/8W	10%	172031000
R107	CACP	1000	1/8W	10%	172031000
R108	CACP	8.2k	1/8W	10%	172038200
R109	CACP	8.2k	1/8W	10%	172038200
R110	CACP	47k	1/8W	10%	172044700
R111	CACP	47k	1/8W	10%	172044700
R112	MEOX	1000	1/4W	5%	195631000
R113	CACP	33k	1/8W	10%	172043300
R114	CACP	100k	1/8W	10%	172051000
R115	CACP	33k	1/8W	10%	172043300
R116	CACP	33k	1/8W	10%	172043300
R123	CACP	10k	1/8W	10%	172041000
C1	ESTM	.22	100V	10%	225452200
C2	ESTM	.047	100V	10%	225444700
C3	TANW	330	6V	20%	265283300
C4	CERM	3.3p	200V	15%	240603300
C5	ESTM	.22	100V	10%	225452200
C6	TANW	47	6V	20%	265274700
C7	CERM	150p	500V	20%	241321500
C8	CERM	15p	500V	20%	241311500
C9	ESTM	.47	63V	10%	225154700
C10	CERM	2.2p	200V	15%	240602200
C11	ESTM	.47	63V	10%	225154700
C12	ALME	220	16V	-20% +100%	273382200
C13	ALME	2200	10V	-10% +100%	273192200
C14	ALME	470	40V	-10% +100%	273784700
C15	ALME	470	40V	-10% +100%	273784700
C16	ALME	22	40V	-10% +100%	273772200
C17	TANW	15	20V	20%	265871500
C18	TANW	15	20V	20%	265871500
C19	ESTM	0.47	63V	10%	225154700
C20	CERM	33p	500V	20%	241313300
C21	PTFE	.1	100V	2%	208950001
C22	TANW	15	20V	20%	265871500
C23	ESTM	10	63V	20%	219971000
C24	CERM	470p	500V	20%	241324700
C25	CERM	150p	500V	20%	241321500
C26	CERM	150p	500V	20%	241321500
C27	CERM	15p	500V	20%	241311500
C28	TANW	15	20V	20%	265871500

Cct Ref.	General Description				Solartron Part No.
C29	TANW	15	20V	20%	265871500
C30	CERM	33p	500V	20%	241313300
C31	CERM	15p	500V	20%	241311500
C32	CERM	3.3p	200V	15%	240603300
C33	CERM	15p	500V	20%	241311500
C34 to C38	CERM	33p	500V	20%	241313300
C39	CERM	150p	500V	20%	241321500
C40	CERM	150p	500V	20%	241321500
C41	CERM	470p	500V	20%	241324700
C42	CERM	.047	25V	+50% -25%	241944700
C43	CERM	470p	500V	20%	241324700
C44	CERM	.047	25V	+50% -25%	241944700
C45	TANW	4.7	35V	20%	266064700
C46 to C48	CERM	1000p	500V	20%	241331000
C49	TANW	4.7	35V	20%	266064700
C50	CERM	0.01	25V	-25% +50%	241941000
C51	CERM	0.01	25V	-25V +50%	241941000
C52	TANW	15	20V	20%	265871500
C54	CERM	3.3p	200V	15%	240603300
C55	CERM	3.3p	200V	15%	240603300
D1	SD3				300522160
D2	SD3				300522160
D3	IN3595				300523590
D4	IN3595				300523590
D5	Zener	12V	.4W	5%	300521480
D6	Zener	12V	.4W	5%	300521480
D7	SD3				300522160
D8	SD3				300522160
D9	SD3				300522160
D10	Zener	3.9V	.4W	5%	300521420
D11	Zener	3.9V	.4W	5%	300521420
D12	W04				300524700
D13	Zener	6.8V	.4W	5%	300522540
D14	W04				300524700
D15	Zener	9.1V	.4W	5%	300521340
D16	Zener	9.1V	.4W	5%	300521340
D17	SD3				300522160
D18	OA47				300520850
D19 to D25	SD3				300522160
D26	Zener	12V	.4W	5%	300521480
D27 to D37	SD3				300522160
D38	IN829	6.2V	1/4W	5%	300525400
D39	Zener	5.1V	.4W	5%	300521310
D40	Zener	6.8V	.4W	5%	300522540
D41	HP5082				300524910
D42	Zener	9.1V	.4W	5%	300521340
D43	Zener	9.1V	.4W	5%	300521340
D44 to D49	SD3				300522160
RV1	CMPM	1M	1/3W	10%	130661000
RV2	CMPM	20k	1/3W	10%	130642000
RV3	CMPM	1000	1/3W	10%	130631000
RV4	CMPM	20k	1/3W	10%	130642000
RV5	CMPM	50k	1/3W	10%	130645000
RV6	CMPM	100	1/3W	10%	130621000
RV7	CMPM	100	1/3W	10%	130621000
RV8	CMPM	50	1/3W	10%	130615000
TR1	40673				300555210
TR2	40673				300555210
TR3	BC107				300553320
TR4	BC107				300553320

Cct Ref.	General Description	Solartron Part No.
TR5	BD166	300555150
TR6	BC107	300553320
TR7	BCY70	300553590
TR8	BD165	300555160
TR9	BD166	300555150
TR10	BC107	300553320
TR11	BCY70	300553590
TR12	MPS-A-13	300554560
TR13	BC107	300553320
TR14	BC107	300553320
TR15	3N163	300554530
TR16	2N4303	300553160
TR17 to TR22	U1899E	300554320
TR23	WD211	300555060
TR24	U1899E	300554320
TR25	3N163	300554530
TR26	BC107	300553320
TR27	BCY70	300553590
TR28	BC107	300553320
TR29	BCY70	300553590
TR30	BC107	300553320
TR31	BCY70	300553590
TR32	BC107	300553320
TR33	BCY70	300553590
TR34	2N2369	300552390
TR35	BCY70	300553590
TR36	BC107	300553320
TR37	BCY70	300553590
TR38	2N2369	300552390
TR39 to TR42	BC107	300553320
TR43	U1899E	300554320
IC1	LM301AH	510000620
IC2	LM301AH	510000620
IC3	LM310H	510090040
IC4	LM301AH	510000620
IC5	LM301AH	510000620
IC6	LM301AH	510000620
IC7	MOS Logic	519600304
IC8	LM308A	510090080
IC9	LM308A	510090080
IC10	SN74LS00N	510002000
IC11	SN74L74N	510001110
X1	Quartz Crystal	300810300
SB	Vertical PV SOcket	352501650
	Horizontal Receptacle	352501700
	Push Button Switch	379601001
	40 Way D.I.L. I.C. Socket	300584880
	Disconnect Crimp	351501070
	Disconnect Pin	355900550

PCB No. 2

Cct Ref.	General Description				Solartron Part No.
*R1	MEFM	9.98M	2W	0.1%	169606702
*R2	MEFM	100.8k	2W	0.1%	
R3	MEFM	18k	1/8W	0.5%	192741802
R4	MEFM	180	1/8W	0.5%	192721802
R5	CACP	1000	1/8W	10%	172031000
R6	PRWW	9.975k	1/3W	0.1%	160300407
R7	CACP	100	1/8W	10%	172021000
R8	CACP	100k	1W	10%	172551000
R9	CACP	1M	1W	10%	172561000
*R10	MEFM	100k	1/2W	0.1%	
*R11	MEFM	10k	1/2W	0.1%	169606802
*R12	MEFM	990k	2W	0.1%	
R13	MEOX	2.2k	1/4W	5%	195632200
R14	CACP	100k	1W	10%	172551000
*R15	MEFM	16k	1/4W	0.5%	169606101
*R16	MEFM	16.9k	1/4W	0.5%	169606101
R17	MEFM	180	1/8W	0.5%	192721802
R18	MEFM	15k	1/8W	0.5%	192741502
R19	CACP	100k	1/8W	10%	172051000
R20	CACP	100k	1/8W	10%	172051000
R21	MEFM	5.1k	1/16W	1%	192635102
R22	MEFM	5.1k	1/16W	1%	192635102
R23	MEOX	2.2k	1/4W	5%	195632200
R24	MEOX	10k	1/4W	5%	195641000
R25	MEOX	2.2k	1/4W	5%	195632200
R26	MEOX	10k	1/4W	5%	195641000
R27	MEOX	47u	1/4W	5%	195624700
R28	MEOX	220	1/4W	5%	195622200
R29	MEFM	27k	1/8W	0.5%	192742702
R30	CACP	1000	1/8W	10%	172031000
R31	MEFM	27k	1/8W	0.5%	192742702
R32	MEOX	18k	1/4W	5%	195641800
R33	MEOX	18k	1/4W	5%	195641800
R34	MEOX	2.2k	1/4W	5%	195632200
C1	ESTF	.22	400V	20%	226152200
C2	ESTM	22	63V	20%	219972200
C3	ESTM	3.3	63V	20%	219963300
C4	ESTM	3.3	63V	20%	219963300
C5	ESTM	2.2	63V	20%	219962200
C6	CERM	33p	500V	20%	241313300
C7	CERM	100p	500V	20%	241321000
C8	CERM	100p	500V	20%	241321000
C9	CERM	470p	1500V	20%	208450090
C10	ESTM	0.047	100V	10%	225444700
C11	CERM	0.047	25V	+50% -25%	241944700
C12	CERM	0.047	25V	+50% -25%	241944700
D3 to D6	HP 5082-6221				300525380
D7	Zener	3.9V	.4W	5%	300521420
D8	Zener	3.9V	.4W	5%	300521420
D9	Zener	3.9V	.4W	5%	300521330
D10	SD3				300522160
D11	SD3				300522160
RV1	CMPM	20k	1/3W	10%	130642000
RV2	CMPM	200	1/3W	10%	130622000
RV3	CMPM	200	1/3W	10%	130622000
RV4	CMPM	500	1/3W	10%	130625000
RV5	CMPM	50	1/3W	10%	130615000
RV6	CMPM	50	1/3W	10%	130615000
TR1	BCY 70				300553590
TR2	BC 107				300553320
TR3	BC 107				300553320
IC1	LM 310H				510090040
IC2	LM 301AH				510000620

*Absolute Match

Cct Ref.	General Description	Solartron Part No.
SA	Switch 5 Wafer 2 Pole 4 Way	379609202
RLB	Relay* 90	301201902
RLC	Relay* 90	301201902

* Two Pole Change Over

Washer 8 BA Small	411000040
Vertical P.V. Socket	352501650

PCB No. 3

Cct Ref.	General Description				Solartron Part No.
R1 to R6	CACP	1000	1/8W	10%	172031000
R7 to R12	CACP	390	1/8W	10%	172023900
R13 to R19	CACP	47	1/8W	10%	172014700
R20	CACP	100	1/8W	10%	172021000
R21 to R28	CACP	10k	1/8W	10%	172041000
R29	CACP	47	1/8W	10%	172014700
D1 to D5	FLV 100				300750030
TR1 to TR6	2N2906A				300554500
TR7 to TR20	BC107				300553320
IC1	LED MAN 101A				300730260
IC2 to IC6	LED MAN 10A				300730250
	14 PIN D.I.L. SOCKET				300584680
	POST				355500980
	TRANSISTOR PAD				300584290

MAIN ASSEMBLY

Cct Ref.	General Description	Solartron Part No.
T1	Mains Transformer	309606904
	Mains Lead	480140200
	Mains Lead Retainer	354003580
	Fuse Holder	360202000
	Fuse	360103040
	Rubber Boot	16000213
MSP1	Mains Selector Switch	375000500
	Input Terminal (Black)	355100360
	Input Terminal (Green)	355100370
	Input Terminal (Red)	355100380
	Guard Link	16200102

ACCESSORIES

Cct Ref.	General Description	Solartron Part No.
	Input Lead Assy (Red)	359900120
	Input Lead Assy (Black)	359900130
	Test Prod Black	351901030
	Test Prod Red	351901040
	Crocodile Clip	355900150
	Cable, E-Z. Hook to Banana Plug (Red)	359900110
	Cable, E-Z. Hook to Banana Plug (Black)	359900100
	Polythene Bag	810000160
	Fuse 150mA	360103040
	Fuse 300mA	360103170

SECTION 6 Specifications

This section contains a copy of the technical specification applicable to this instrument.

This instrument is designed and manufactured to a higher specification than is claimed commercially. In order that that the user may benefit as appropriate, this technical manual may relate to a superior performance. In the event of contradictions between specifications, no additional claims are made for the instrument above that claimed in the current data sheet.

General

Display

Type:	7 Bar Red Light emitting diodes
Scale Length:	109,999 max.
Polarity Indication:	Displayed for negative dc inputs
Overload Indication:	DC/AC/μA flashing 1, Ω steady 1
Annunciator:	mV, V, μA, Ω, kΩ.
Ranging:	Automatic, redundant leading zeros are blanked.

Environment

Working Temperature Range	0 to +45°C
Storage Temperature Range	−30 to +70°C
Maximum Relative Humidity	70% at 40°C

Power Supply

Voltage:	115V/230V + 10% −15%
Frequency:	50Hz ±1% or 60Hz ±1%
Consumption:	12VA
Fuses:	230V 150mA Slo Blo 115V 300mA Slo Blo

Size

Width:	216mm	(8.5in)
Height:	89mm	(3.5in)
Depth:	280mm	(11in)
Weight:	2.73kg	(6 lb)

DC VOLTAGE (VDC)		Limits of Error				
		24 hours at 23°C ±1°C		90 days within 23°C ±5°C		T.C. of errors 0°C to 45°C
Range	Input Resistance	±% of Reading	±% of Range	±% of Reading	±% of Range	per °C
10μV to 1.10000V	>1000MΩ	0.005	0.002	0.02	0.003	<10 ppm ±2μV
100μV to 11.0000V	>1000MΩ	0.005	0.002	0.02	0.003	<10 ppm
1mV to 110.000V	10.1MΩ	0.005	0.002	0.035	0.003	<20 ppm ±0.2 digits
10mV to 1000.00V	10.1MΩ	0.01	0.002	0.04	0.003	<20 ppm

All ranges protected to 1000V DC or 240V r.m.s. applied continuously.

Reading time: approx. 3 per second
Ranging time: approx. 1 second

AC VOLTAGE (VAC)		Limits of Error				
		24 hours at 23°C ±1°C		90 days within 23°C ±5°C		T.C. of errors 0°C to 45°C
Range	Input Impedance	±% of Reading	±% of Range	±% of Reading	±% of Range	per °C
10μV to 1.10000V	1MΩ 100p	0.1	0.01	0.15	0.02	<50 ppm ±0.4 digits
100μV to 11.0000V	1MΩ 100p	0.2	0.01	0.25	0.02	<150 ppm ±0.4 digits
1mV to 110.000V	1MΩ 100p	0.2	0.01	0.25	0.02	<150 ppm ±0.4 digits
10mV to 750.00V	1MΩ 100p	0.2	0.01	0.3	0.02	<150 ppm ±0.4 digits

Measurement is mean sensing, r.m.s. calibrated assuming a pure sine wave input.
Frequency Range: 40Hz to 10kHz
(500V max above 1kHz)

All ranges protected to 1100V peak AC or 250V DC

Reading Rate: approx. 2 per second
Ranging Time: approx. 3 seconds

RESISTANCE (Ω)		Limits of Error				
		24 hours at 23°C ±1°C		90 days within 23°C ±5°C		T.C. of errors 0°C to 45°C
Range	Current Through R	±% of Reading	±% of Range	±% of Reading	±% of Range	per °C
100mΩ to 11.0000kΩ	100μA	0.05	0.005	0.1	0.005	<50 ppm ±20mΩ
1Ω to 110.000kΩ	100μA	0.05	0.005	0.1	0.005	<50 ppm
10Ω to 1100.00kΩ	1μA	0.05	0.005	0.1	0.005	<50 ppm
100Ω to 11000.0kΩ	1μA	0.25	0.005	0.3	0.005	<50 ppm

All ranges protected to 200V DC or 200V r.m.s. AC.

Reading time: approx. 3 per second
Ranging time: approx. 1 second

DC CURRENT (μADC)		Limits of Error				
		24 hours at 23°C ±1°C		90 days within 23°C ±5°C		T.C. of errors 0°C to 45°C
Range	Input Resistance	±% of Reading	±% of Range	±% of Reading	±% of Range	per °C
1nA to 110.000μA	<100Ω	0.05	0.005	0.1	0.005	<50 ppm ±0.2nA
10nA to 1100.00μA	<100Ω	0.05	0.005	0.1	0.005	<50 ppm

All ranges protected to 100V

Reading time: approx. 3 per second
Ranging time: approx. 1 second

Common Mode Rejection

Measured with an imbalance of 1kΩ in the input leads
Maximum Common Mode Voltage: 500V dc or peak ac

DC Measurement: Rejection of dc > 120dB
Rejection of 50/60Hz ± 1% > 120dB
AC Measurement: Rejection of dc > 120dB
Rejection of 50/60Hz ± 1% > 40dB

Series Mode Rejection

Ratio of peak interference to 1 digit reading error, produced

DC Measurements: Rejection of 50/60Hz ± 1% > 60dB

APPENDIX

This section contains specialised selection procedures and/or test equipment to facilitate servicing.

CONTENTS

	Page
FET Selection Procedure	A2
Setting Up Case 70502	A3

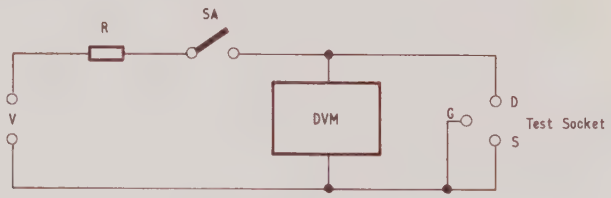
FET SELECTION PROCEDURE

PURPOSE

To select four FET's type U1899E with Ron matched to within 1Ω at a drain-source current of 100μA.

TEST PROCEDURE

The following test procedure should be carried out using the test circuit shown below or Solartron Test Equipment TG1100/1.



TEST CIRCUIT

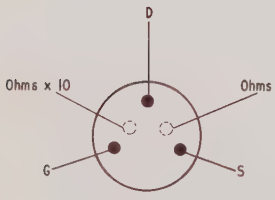
$$\left.\begin{array}{l} V = 10V \\ R = 100k \end{array}\right\} \quad \frac{V}{R} = 100\mu A \pm 0.2\%$$

(a) Devices to be tested should be allowed to settle to the ambient temperature of the chamber in which the matching operation is to be done.
This temperature should be $23^{o}C \pm 1^{o}C$.

(b) Place the device under test in the test socket using tweezers or pliers to ensure that its temperature is not raised by handling.

(c) Press switch SA and note DVM reading.
Use the relation 1mV = 10Ω to calculate the Ron value.

(d) Mark the top of the device with two coloured dots of paint as shown in following view employing the standard colour code.
Ron to be given to nearest whole number, e.g.



TOP VIEW

45.6Ω	YELLOW-BLUE
46.3Ω	YELLOW-BLUE
46.5Ω	YELLOW-VIOLET

(e) Select sets of four devices, each with the same colour code.

COLOUR CODE

0	Black
1	Brown
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
7	Violet
8	Grey
9	White

SETTING-UP CASE 70502

INTRODUCTION

In order to achieve the greatest accuracy during a calibration it is essential that the operating temperatures affecting circuit components are as near as possible to those experienced within the instrument case during normal operation.

The Setting-Up Case 70502 enhances the calibration accuracy by allowing access for adjustments whilst the instrument is functioning under normal working conditions.

GENERAL DESCRIPTION

The Setting-Up Case is basically a normal instrument case with holes drilled in convenient positions allowing access to the potentiometers. Fig. A1 shows the side view of the Case with the access holes and the relevant potentiometers.

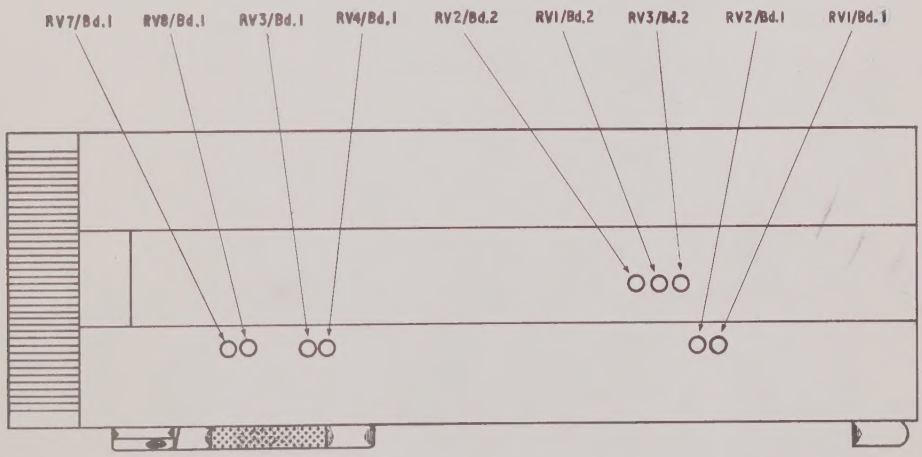


Fig. A.1. View of Setting-Up Case showing potentiometer access holes.

MP MASTER
MA24044